
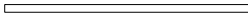

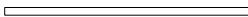


8S650GXM-P Schematics

Revision 2.0

Dte: 92/09/18

SHEET	TITLE
1	COVER SHEET
2	BOM & PCB MODIFY HISTORY
3	BLOCK DIAGRAM
4,5,6	INTEL CPU_WMT_478
7-10	SIS651/645DX (NORTH BRIDGE) HOST; DDR; AGP, HYPER ZIP
11-14	962 (SOUTH BRIDGE)
15	CKG(ICS952004) + CKBF (ICS93722)
16,17	DDR SDRAM DIMMS 1,2 & DDR TERMINATION
18	AGP SLOT
19	VGA Connector
20	PCI SLOT 1-3
21	IDE, USB
22	Winbond W83697HF
23	BIOS
24	COM, PRT, FDD, KB/MS, IR
25	CNR SLOT
26	AUDIO AC 97 CODEC
27	AUDIO JACK, GAME PORT
28	RTL8100B & USB CONNECTOR
29	PANEL, STR LED, FANS, CPU GN
30	VCORE PHASE PWM HIP 6301 + 6601
31	ALL POWER CIRCUIT
32	ATX & ATX12V CONN
33	GPIO Connection
34	TEST POINT

 COMPONENT SIDE (1 oz. Copper)		
 GND SIDE (1 oz. Copper)		
 VCC SIDE (1 oz. Copper)		
 SOLDER SIDE (1 oz. Copper)		
GIGABYTE		
COVER SHEET		
Title		
Size	Document Number	Rev
Custom	GA-8S650GXM-P	2.0
Date:	星期三, 十二月 03, 2003	Sheet 1 of 32

Model Name: 8S650GXM-P

Version:2.0

Circuit or PCB layout change
for next version

Component value change
history

AUTOBOM
2003/09/08

Date	Change Item	Reason
09/08	RELAYOUT REV:1.01	FOR PRESCOTT CPU
09/10	BOM	R467 1.05k/6/1 change to 931/6/1
09/17	BOM	CHANG U14 TO ISA FLASH ROM
09/18	BOM	CHANG PCB FROM 1.01 TO 1.02
10/02	BOM	REMOVE YUFO PCB
10/07	BOM	REMOVE TH PCB AND HAVE A NEW BOM
10/23	BOM	CHANGE PCB SILKSCREEN MODEL NAME TO 8S650GXM
11/06	BOM	FIX YF PCB FAIL ,R636 CHANGE TO 34/6/1,R639 CHANGE TO 90.9/6/1
11/17	BOM	CHANGE FB40,FB41 TO 0 OHM

Date	Change Item	Reason
09/18	RELAYOUT REV:1.02	FOR FACTORY MANUFACTURE

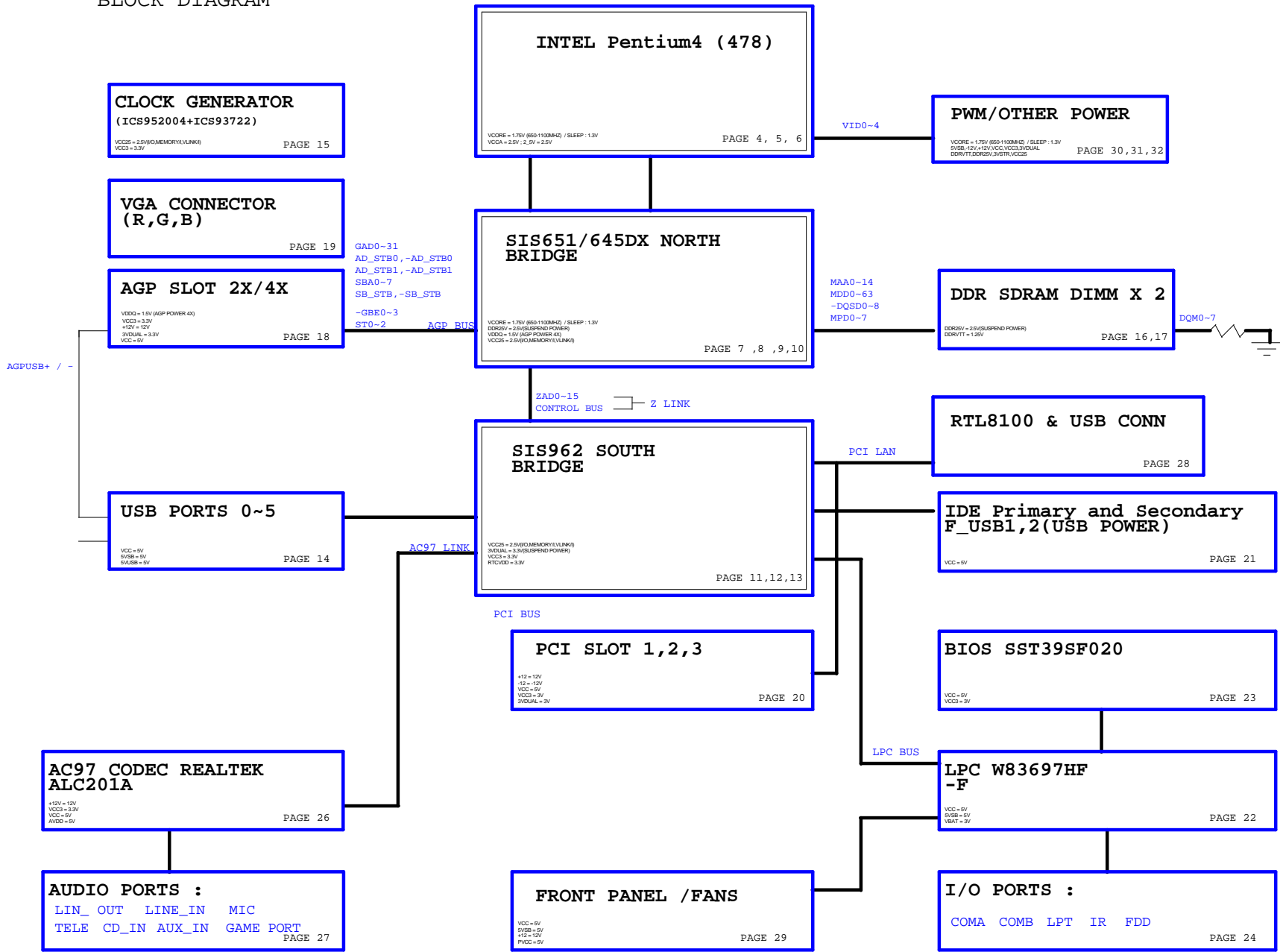
GIGABYTE

BOM & PCB MODIFY HISTORY

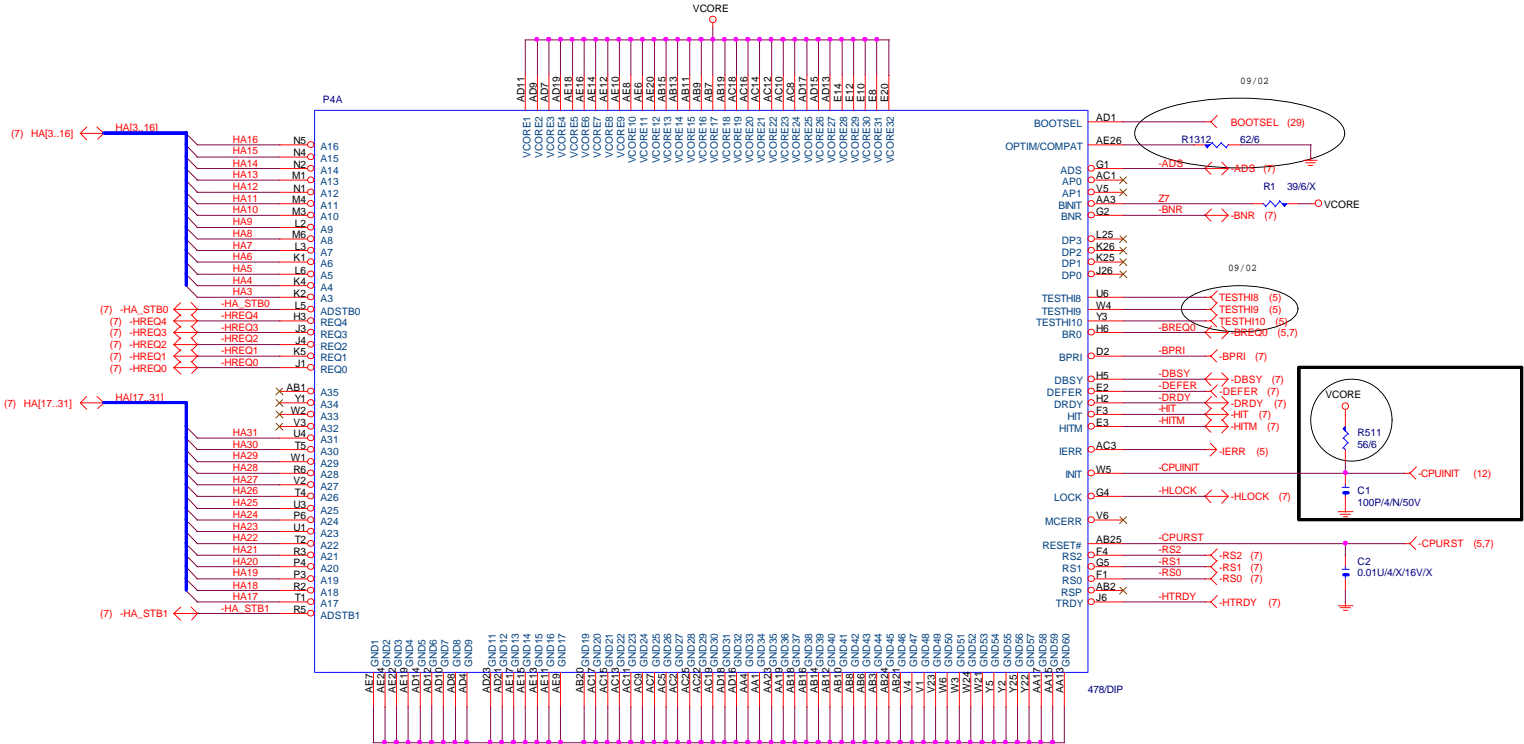
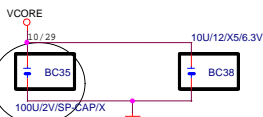
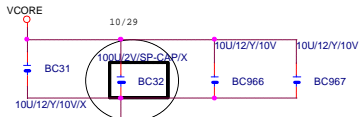
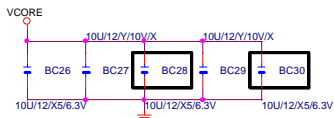
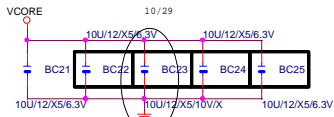
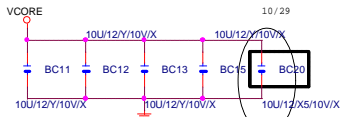
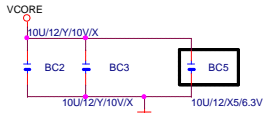
Title			Rev
Document Number			1.0
Date: 星期日, 十二月 03, 2003			Sheet 2 of 32

GA-8S650GXM-P

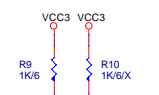
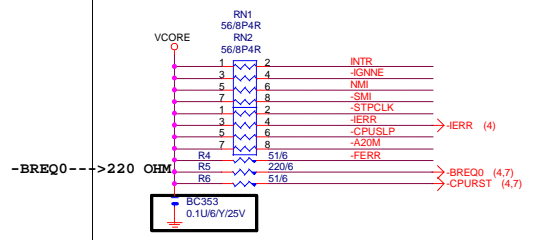
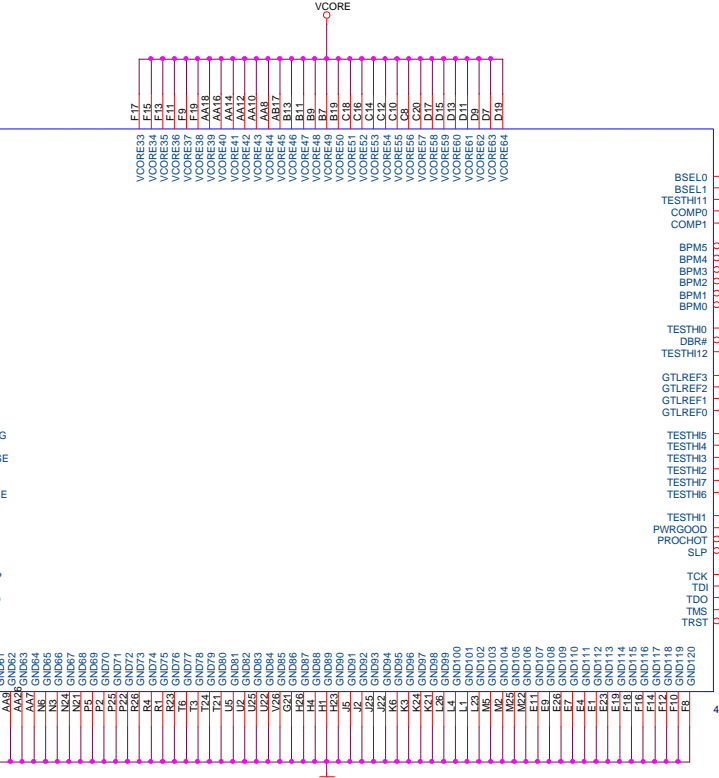
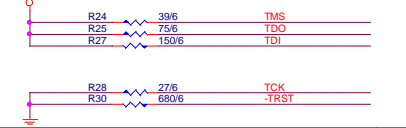
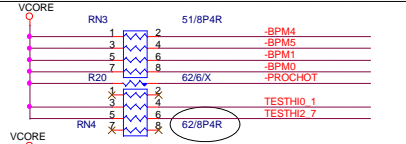
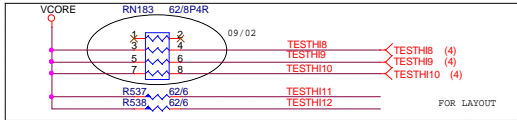
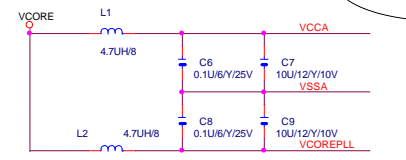
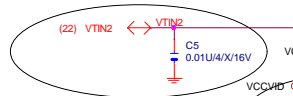
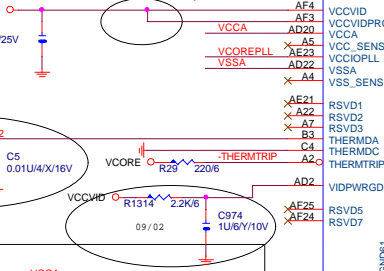
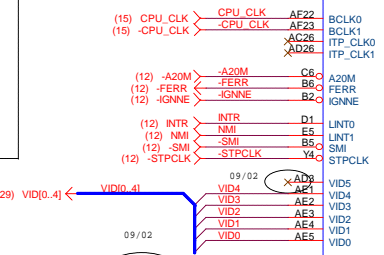
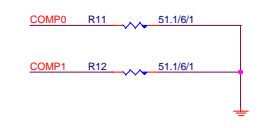
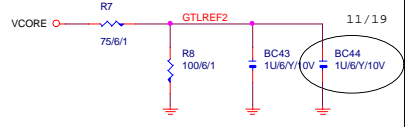
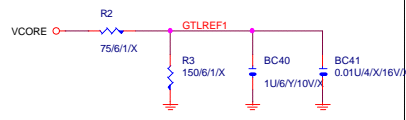
BLOCK DIAGRAM



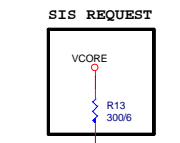
(X5R) X11 1206(10U) NOTE:GIGA



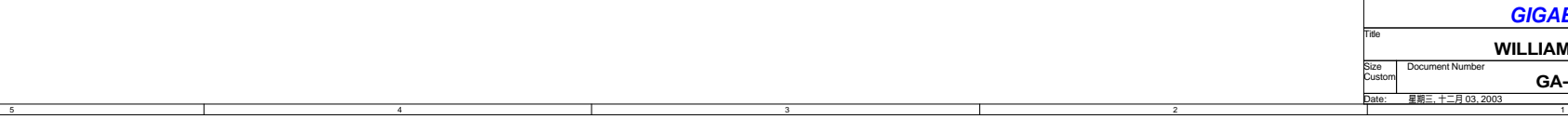
GIGABYTE		
WILLIAMATE 478A		
Title	Document Number	Rev
Size Custom	GA-8S650GXM-P	2.0
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BSELO --->100/133



Title		GIGABYTE	
Document Number		WILLIAMATE 478B	
Size	Custom	Document Number	GA-8S650GXM-P
Date:	Rev	Sheet	2.0
日期: 2003.03.12	Rev	5	2



GIGABYTE			
WILLIAMATE 478C			
Title	Document Number		
Size	GA-8S650GXM-P		Rev 2.0
Custom			
Date:	星期二, 十二月 03, 2003	Sheet 6	of 32

-DBI[0..3] <-> DBI[0..3] (6)
 HD[0..63] <-> HD[0..63] (6)
 HA[3..31] <-> HA[3..31] (4)
 GD[0..31] <-> GD[0..31] (18)
 SBA[0..7] <-> SBA[0..7] (18)
 ST[0..2] <-> ST[0..2] (18)

(15) HCLK <-> HCLK A126 CPUCCLK
 (15) HCLK <-> HCLK AH28 CPUCCLK#
 (4) HLOCK <-> HLOCK U24 HLOCK#
 (4) DEFER <-> DEFER U26 DEFER#
 (4) HTRDY <-> HTRDY V26 HTRDY#
 (4.5) CPURST <-> CPURST D19 CPURST#
 (5) CPUFWOK <-> CPUFWOK CPUFWOK#
 (4) BPR1 <-> BPR1 T27 BPR#
 (4.5) BREQ0 <-> BREQ0 U25 BREQ0#
 (4) RS2 <-> RS2 T24 RS#2
 (4) RS1 <-> RS1 T26 RS#1
 (4) RS0 <-> RS0 U29 RS#0
 (4) ADS <-> ADS V28 ADS#
 (4) HITM <-> HITM T28 HITM#
 (4) HIT <-> HIT U28 HIT#
 (4) DRDY <-> DRDY W26 DRDY#
 (4) DBSY <-> DBSY V24 DBSY#
 (4) BNR <-> BNR V27 BNR#
 (4) HREQ4 <-> HREQ4 W28 HREQ#4
 (4) HREQ3 <-> HREQ3 W29 HREQ#3
 (4) HREQ2 <-> HREQ2 W24 HREQ#2
 (4) HREQ1 <-> HREQ1 W25 HREQ#1
 (4) HREQ0 <-> HREQ0 Y27 HREQ#0
 (4) HA_STB1 <-> HA_STB1 AD24 HASTB#1
 (4) HA_STB0 <-> HA_STB0 AA24 HASTB#0

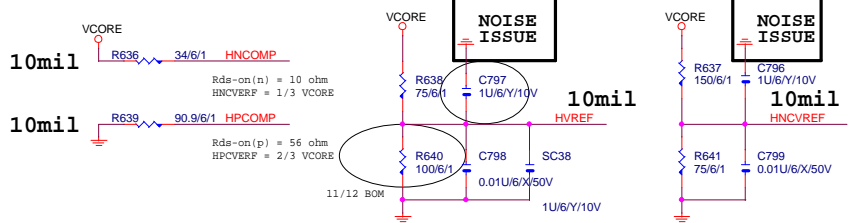
HA31 AF26 HA#31
 HA30 AE25 HA#30
 HA29 AH28 HA#29
 HA28 AD26 HA#28
 HA27 AG29 HA#27
 HA26 AE26 HA#26
 HA25 AF28 HA#25
 HA24 AC24 HA#24
 HA23 AG28 HA#23
 HA22 AE29 HA#22
 HA21 AD28 HA#21
 HA20 AC25 HA#20
 HA19 AD27 HA#19
 HA18 AE26 HA#18
 HA17 AF27 HA#17
 HA16 AB24 HA#16
 HA15 AB26 HA#15
 HA14 AC28 HA#14
 HA13 AC26 HA#13
 HA12 AC29 HA#12
 HA11 AA26 HA#11
 HA10 AB28 HA#10
 HA9 AB27 HA#9
 HA8 AA25 HA#8
 HA7 AA23 HA#7
 HA6 AA28 HA#6
 HA5 Y26 HA#5
 HA4 Y24 HA#4
 HA3 Y28 HA#3



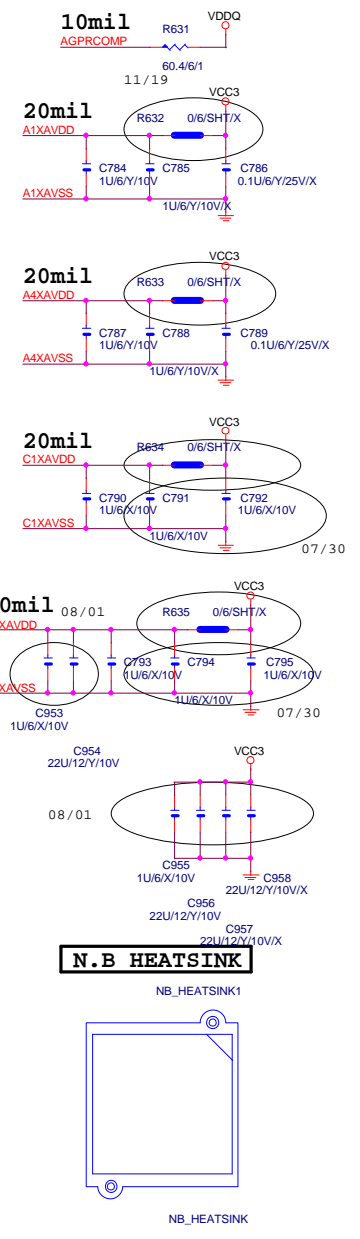
651/645DX-1

HOST

AGP



VREF C-CAP PULL-UP MEASURE NOISE WORST.



GIGABYTE		
SIS651/645DX(HOST/AGP)		
Title	Document Number	Rev
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MDDI0_631 ← MDDI[0:63] (16,17)
 DQMIO_71 → DQM[0..7] (16,17)
 MAAI0_141 → MAA[0..14] (16,17)
 -CSI0_31 → -CS[0..3] (16,17)
 -CKE0_51 → -CKE[0..5] (16)
 -DQSDI0_71 → -DQS[0..7] (16,17)

DDR MD DAMPING

Near DIMM 1

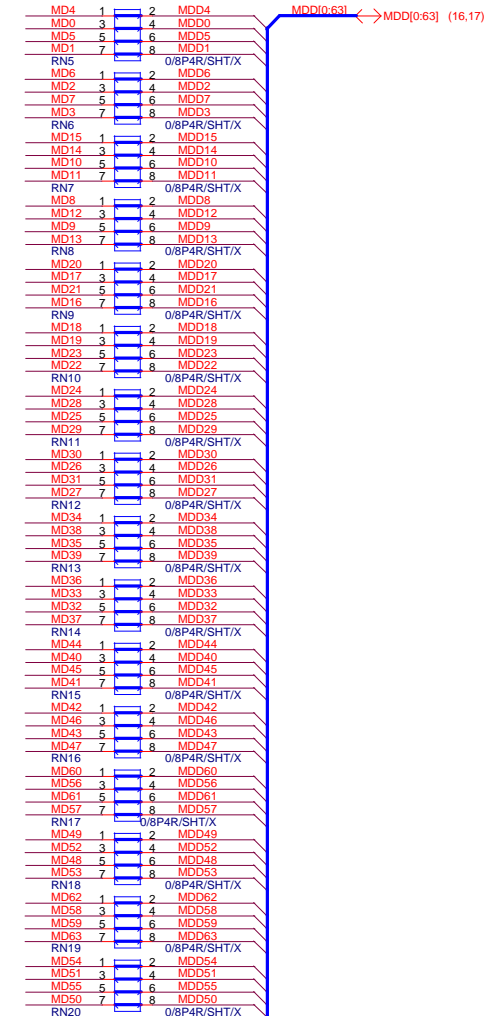
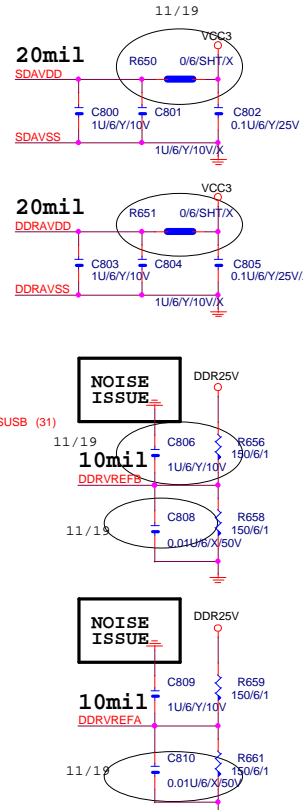
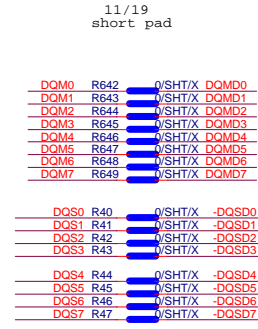
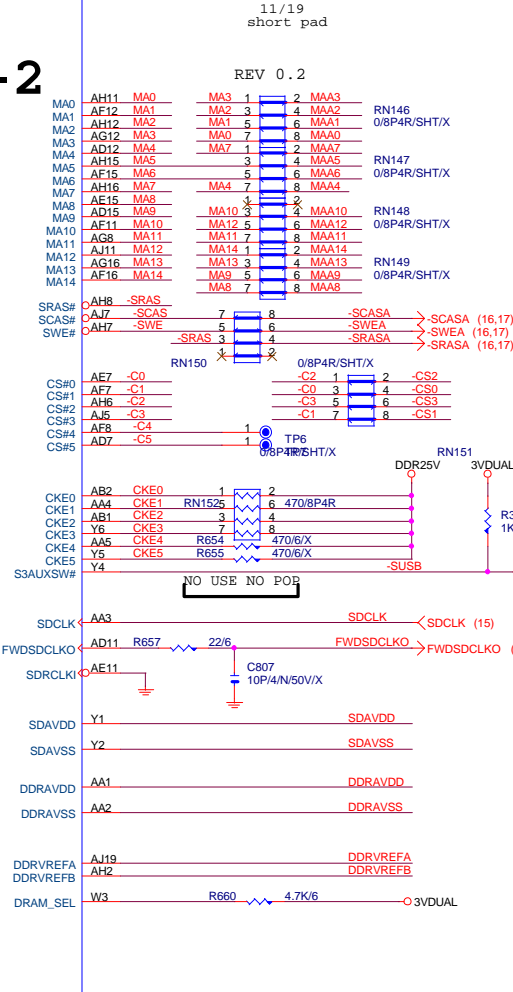
11/19 short pad

MD0	AJ23	MD0
MD1	AG22	MD1
MD2	AH21	MD2
MD3	AJ21	MD3
MD4	AD23	MD4
MD5	AE23	MD5
MD6	AF22	MD6
MD7	AF21	MD7
DQMD0	AD22	MD7
DQS0	AH22	DQM0
MD8	AD21	MD8
MD9	AG20	MD9
MD10	AE19	MD10
MD11	AF18	MD11
MD12	AE21	MD12
MD13	AD20	MD13
MD14	AD19	MD14
MD15	AH19	MD15
DQMD1	AF20	MD15
DQS1	AH20	DQM1
MD16	AF18	MD16
MD17	AG18	MD17
MD18	AH17	MD18
MD19	AD16	MD19
MD20	AD18	MD19
MD21	AD17	MD20
MD22	AF17	MD21
MD23	AJ17	MD22
DQMD2	AJ17	MD23
DQS2	AH18	DQM2
MD24	AD14	MD24
MD25	AG14	MD25
MD26	AJ13	MD26
MD27	AE13	MD26
MD28	AJ15	MD27
MD29	AF14	MD28
MD30	AD13	MD29
MD31	AF13	MD30
DQMD3	AH13	MD31
DQS3	AH14	DQM3
MD32	AD10	MD32
MD33	AH10	MD33
MD34	AE9	MD34
MD35	AD8	MD35
MD36	AG10	MD36
MD37	AF10	MD37
MD38	AH9	MD38
MD39	AF9	MD39
DQMD4	AD9	MD39
DQS4	AJ9	DQM4
MD40	AH5	MD40
MD41	AG4	MD41
MD42	AE5	MD42
MD43	AH3	MD43
MD44	AG6	MD44
MD45	AF6	MD45
MD46	AF5	MD46
MD47	AF4	MD47
DQMD5	AH4	MD47
DQS5	AJ3	DQM5
MD48	AE4	MD48
MD49	AD6	MD49
MD50	AC5	MD50
MD51	AG5	MD51
MD52	AG2	MD52
MD53	AG1	MD53
MD54	AF3	MD54
MD55	AC6	MD55
DQMD6	AD4	MD55
DQS6	AF2	DQM6
MD56	AB6	MD56
MD57	AD3	MD57
MD58	AE6	MD58
MD59	AB3	MD59
MD60	AC4	MD60
MD61	AE1	MD61
MD62	AD2	MD62
MD63	AC1	MD63
DQMD7	AB4	MD63
DQS7	AC2	DQM7

651
645DX-2

U38B

SIS650GX/B0



GIGABYTE

Title		
SIS651/645DX(DDR)		
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Custom	GA-8S650GX-M-P	2.0
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VREF C-CAP PULL-UP MEASURE NOISE WORST.

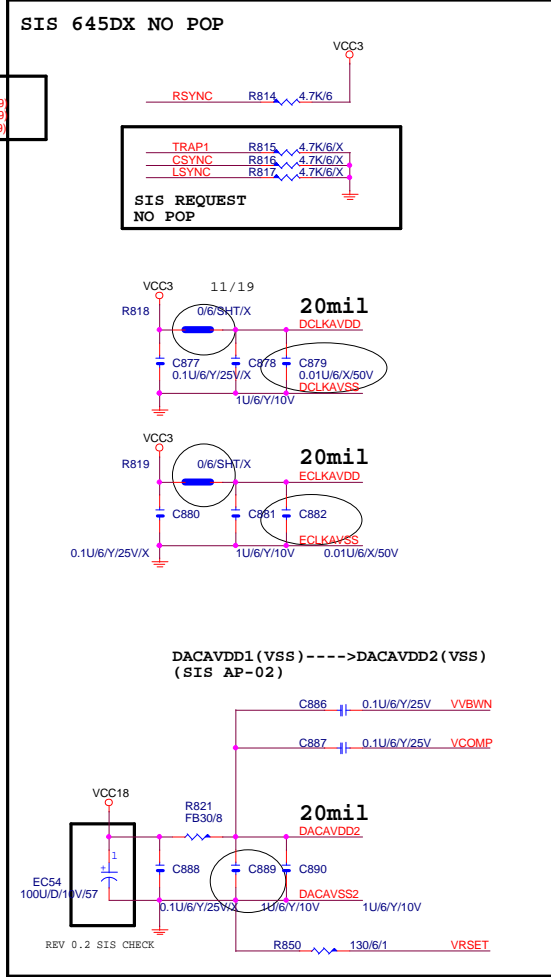
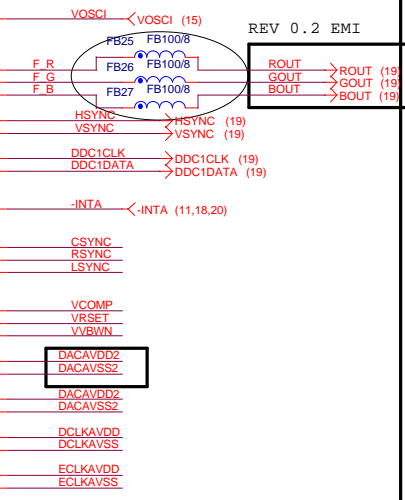
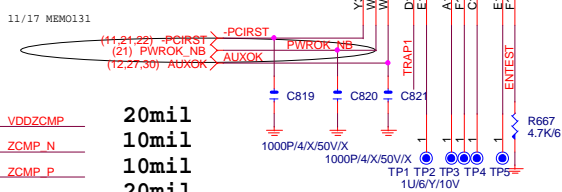
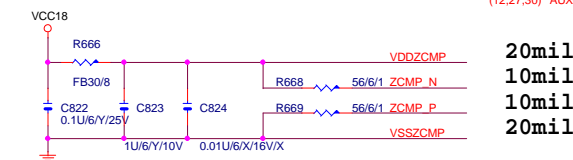
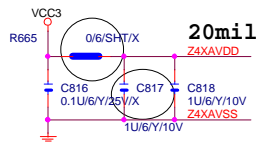
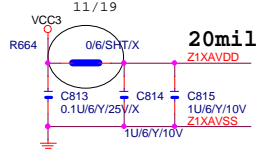
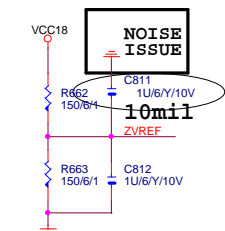
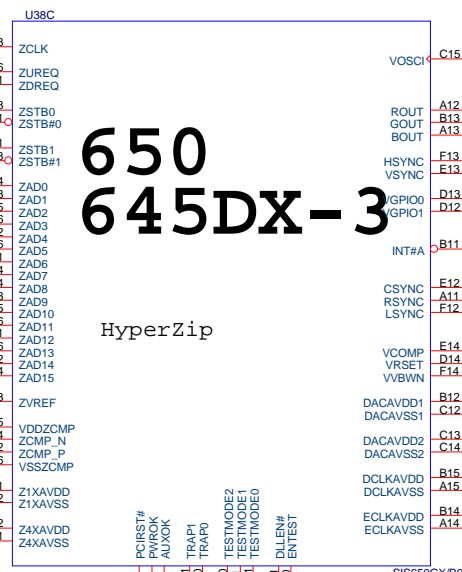
NOTE: This page is for universal PCB design(suitable for both 645 or 650)

NB Hardware Trap Table

	0	1	Default	embedded pull-low (30-50K Ohm)
DLEN#	enable PLL	disable PLL	0	yes
DRAM_SEL	SDR	DDR	1 (DDR)	yes
TRAP0	normal	NB debug mode	0	yes
TRAP1	TV selection, NTSC/PAL(0/1)		0	
CSYNC	enable VB		0	
RSYNC	enable VGA interrupt		1	
LSYNC	enable panel link		0	

650 645DX-3

HyperZip

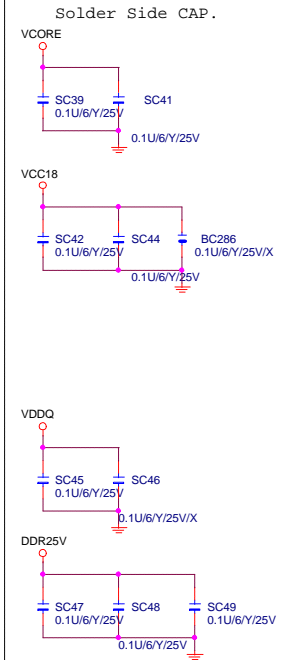
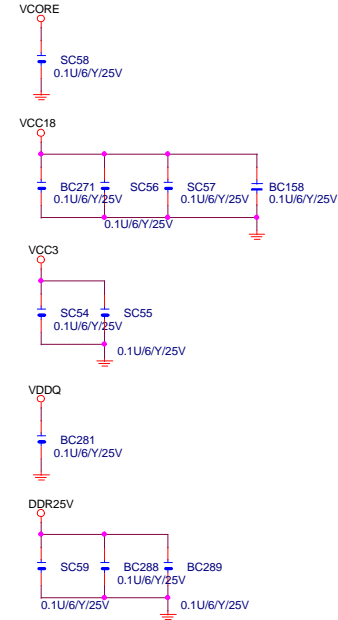
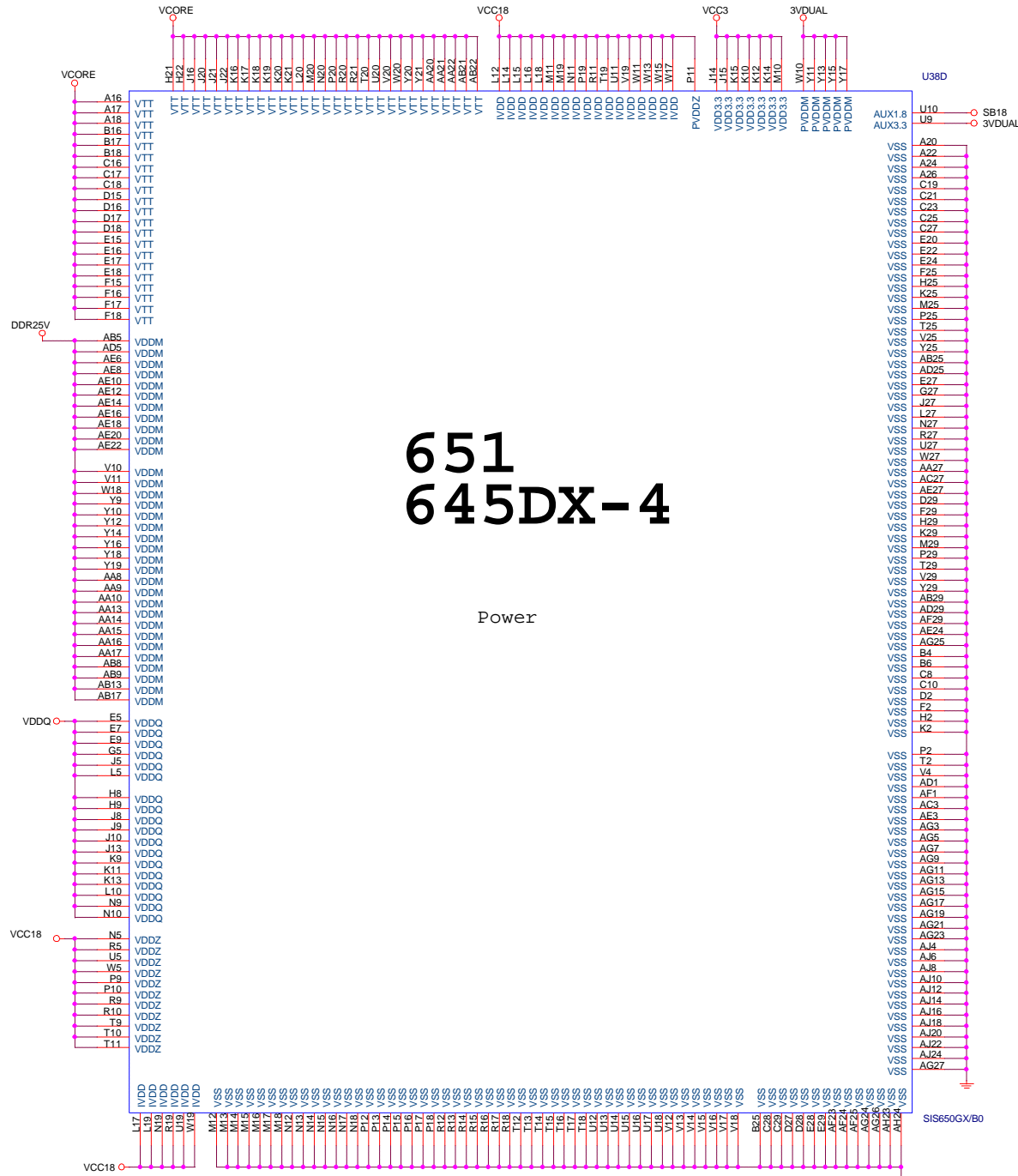


GIGABYTE

Title			SIS651/645DX(HYPER ZIP)		
Size	Document Number	Rev		2.0	
Custom	GA-8S650GXM-P				
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Power



GIGABYTE		
Title SIS651/645DX(PWR)		
Size Custom	Document Number GA-8S650GXM-P	Rev 2.0
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PDD0..15L <-> PDD[0..15] (21)
 SDD0..15L <-> SDD[0..15] (21)
 -REQ0..4L <-> -REQ[0..4] (20)
 -GNT0..3L <-> -GNT[0..3] (20)
 -C_BE0..3L <-> -C_BE[0..3] (20)
 AD0..31L <-> AD[0..31] (20)

-REQ4 F1 PREQ#4
 -REQ3 F2 PREQ#3
 -REQ2 E1 PREQ#2
 -REQ1 H5 PREQ#1
 -REQ0 F3 PREQ#0
 -GNT3 H3 PGNT#4
 -GNT2 G1 PGNT#3
 -GNT1 G2 PGNT#2
 -GNT0 H4 PGNT#1
 -C_BE3 K3 C/BE#3
 -C_BE2 M4 C/BE#2
 -C_BE1 P1 C/BE#1
 -C_BE0 R4 C/BE#0
 (9,18,20) -INTA E3 INT#A
 (18,20) -INTB F4 INT#B
 (20) -INTC E2 INT#C
 (20) -INTD G4 INT#D
 (20) -FRAME M3 FRAME#
 (20) -IRDY M1 IRDY#
 (20) -TRDY M2 TRDY#
 (20) -STOP N4 STOP#
 (20) -SERR M5 SERR#
 (20) PAR N3 PAR
 (20) -DEVSEL N1 DEVSEL#
 (20) -PLOCK N2 PLOCK#
 (15) PCLK_SB Y2 PCICLK
 (9,21,22) -PCIRST R671 PCIRST#
 (15) ZCLK_SB Z2 ZCLK
 (9) ZSTB0 N19 ZSTB0
 (9) -ZSTB0 N20 ZSTB0#
 (9) ZSTB1 K20 ZSTB1
 (9) -ZSTB1 K19 ZSTB1#
 (9) ZREQ_UP N16 ZUREQ
 (9) ZREQ_DN N17 ZDREQ
 -SVDDZCMP R19 VDDZCMP
 -SZCMP_N N18 ZCMP_N
 -SZCMP_P R18 ZCMP_P
 -SVSSZCMP P18 VSSZCMP
 -SZ1XAVDD U20 Z1XAVDD
 -SZ1XAVSS U19 Z1XAVSS
 -SZ4XAVDD T20 Z4XAVDD
 -SZ4XAVSS T19 Z4XAVSS
 -SZVREF R20 ZVREF
 -ZVSSREF P20 ZVSSREF

AD31 L4
 AD30 L4
 AD29 L4
 AD28 L4
 AD27 L4
 AD26 L4
 AD25 L4
 AD24 L4
 AD23 L4
 AD22 L4
 AD21 L4
 AD20 L4
 AD19 L4
 AD18 L4
 AD17 L4
 AD16 L4
 AD15 L4
 AD14 L4
 AD13 L4
 AD12 L4
 AD11 L4
 AD10 L4
 AD9 L4
 AD8 L4
 AD7 L4
 AD6 L4
 AD5 L4
 AD4 L4
 AD3 L4
 AD2 L4
 AD1 L4
 AD0 L4

PCI

IDE

962/961B

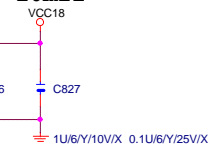
HyperZip

ZAD0 M18 ZAD0
 ZAD1 M17 ZAD1
 ZAD2 M16 ZAD2
 ZAD3 M16 ZAD3
 ZAD4 M16 ZAD4
 ZAD5 M16 ZAD5
 ZAD6 M16 ZAD6
 ZAD7 M16 ZAD7
 ZAD8 M16 ZAD8
 ZAD9 M16 ZAD9
 ZAD10 M16 ZAD10
 ZAD11 M16 ZAD11
 ZAD12 M16 ZAD12
 ZAD13 M16 ZAD13
 ZAD14 M16 ZAD14
 ZAD15 M16 ZAD15
 M18 ZAD0
 M17 ZAD1
 M16 ZAD2
 M16 ZAD3
 M16 ZAD4
 M16 ZAD5
 M16 ZAD6
 M16 ZAD7
 M16 ZAD8
 M16 ZAD9
 M16 ZAD10
 M16 ZAD11
 M16 ZAD12
 M16 ZAD13
 M16 ZAD14
 M16 ZAD15

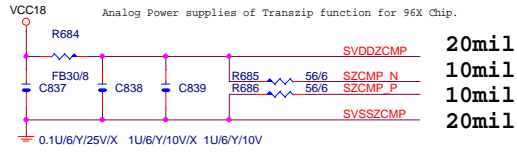
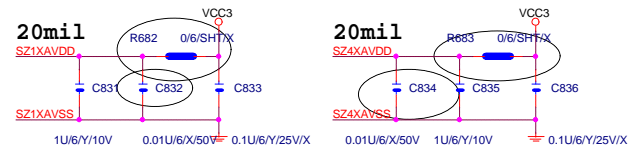
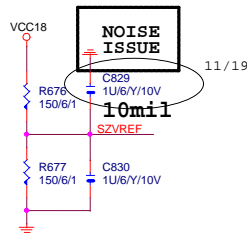
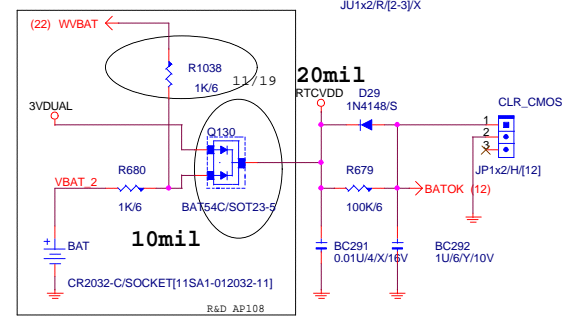
(9) ZAD[0..15] <-> ZAD[0..15]

IDEAVDD Y3
 IDEAVSS Y4
 ICHRDYA W10 PDIORDY <-> PDIORDY (21)
 IDREQA Y11 PDDREQ <-> PDDREQ (21)
 IIRQA Y12 P66DET <-> P66DET (21)
 CBLIDA U12
 IIOR#A Y11 -PDIOR <-> -PDIOR (21)
 IIOW#A Y9 -PDIOW <-> -PDIOW (21)
 IDACK#A Y10 -PDDACK <-> -PDDACK (21)
 IDSA#A T11 PDA2 <-> PDA2 (21)
 IDSA#A U11 PDA1 <-> PDA1 (21)
 IDSA#A W11 PDA0 <-> PDA0 (21)
 IDECSA#1 T12 -PDCS3 <-> -PDCS3 (21)
 IDECSA#0 Y12 -PDCS1 <-> -PDCS1 (21)
 ICHRDYB W17 SIORDY <-> SIORDY (21)
 IDREQB Y17 SDDREQ <-> SDDREQ (21)
 IIRQB T16 IRQ15 <-> IRQ15 (21)
 CBLIDB U17 S66DET <-> S66DET (21)
 IIOR#B T14 -SDIOR <-> -SDIOR (21)
 IIOW#B W16 -SDIOW <-> -SDIOW (21)
 IDACK#B Y16 -SDDACK <-> -SDDACK (21)
 IDSA#B Y18 SDA2 <-> SDA2 (21)
 IDSA#B T15 SDA1 <-> SDA1 (21)
 IDSA#B U17 SDA0 <-> SDA0 (21)
 IDECSB#1 U16 -SDCS3 <-> -SDCS3 (21)
 IDECSB#0 W18 -SDCS1 <-> -SDCS1 (21)
 IDA0 U10 PDD0
 IDA1 W8 PDD2
 IDA2 T9 PDD3
 IDA3 Y7 PDD4
 IDA4 Y7 PDD5
 IDA5 Y6 PDD6
 IDA6 Y5 PDD7
 IDA7 W6 PDD8
 IDA8 U8 PDD9
 IDA9 W7 PDD10
 IDA10 Y8 PDD11
 IDA11 U8 PDD12
 IDA12 Y8 PDD13
 IDA13 T10 PDD14
 IDA14 W9 PDD15
 IDA15
 IDB0 Y16 SDD0
 IDB1 V15 SDD1
 IDB2 U14 SDD2
 IDB3 W14 SDD3
 IDB4 Y13 SDD4
 IDB5 T13 SDD5
 IDB6 Y13 SDD6
 IDB7 Y12 SDD7
 IDB8 W12 SDD8
 IDB9 W13 SDD9
 IDB10 Y14 SDD10
 IDB11 V14 SDD11
 IDB12 W15 SDD13
 IDB13 Y15 SDD14
 IDB14 U15 SDD15
 IDB15

20mil



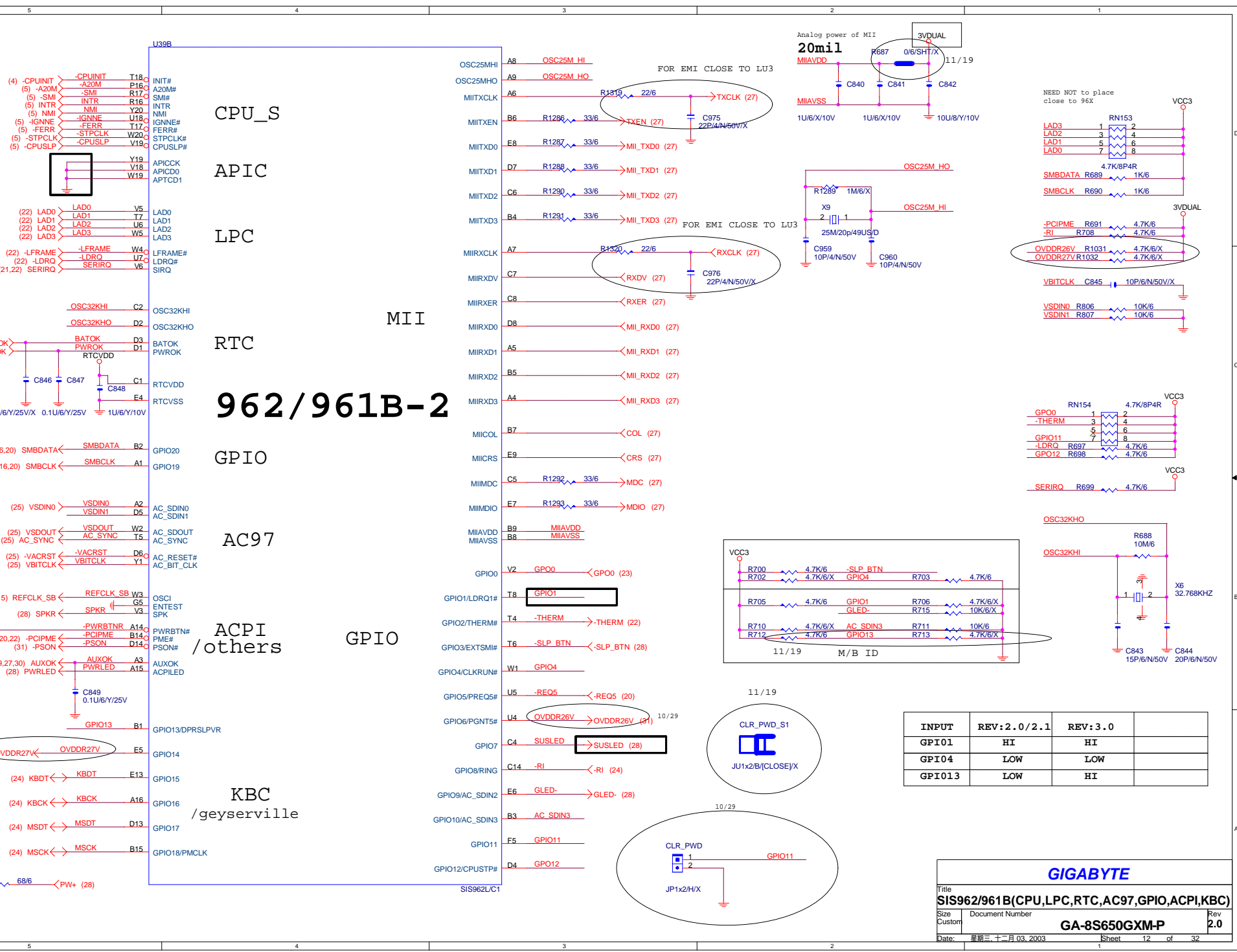
CLR_CMOS	CLEAR COMS JUMPER
1-2	Enable
2-3	Normal (Default)



Analog Power supplies of Transzip function for 96X Chip.

NF REQUEST CLR_CMOS

GIGABYTE		
SIS962(HP ZIP,PCI,IDE)		
Title		
Size	Document Number	Rev
Custom		2.0
GA-8S650GXM-P		
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CPU_S

APIC

LPC

MII

RTC

962/961B-2

GPIO

AC97

ACPI
/others

GPIO

KBC
/geyserville

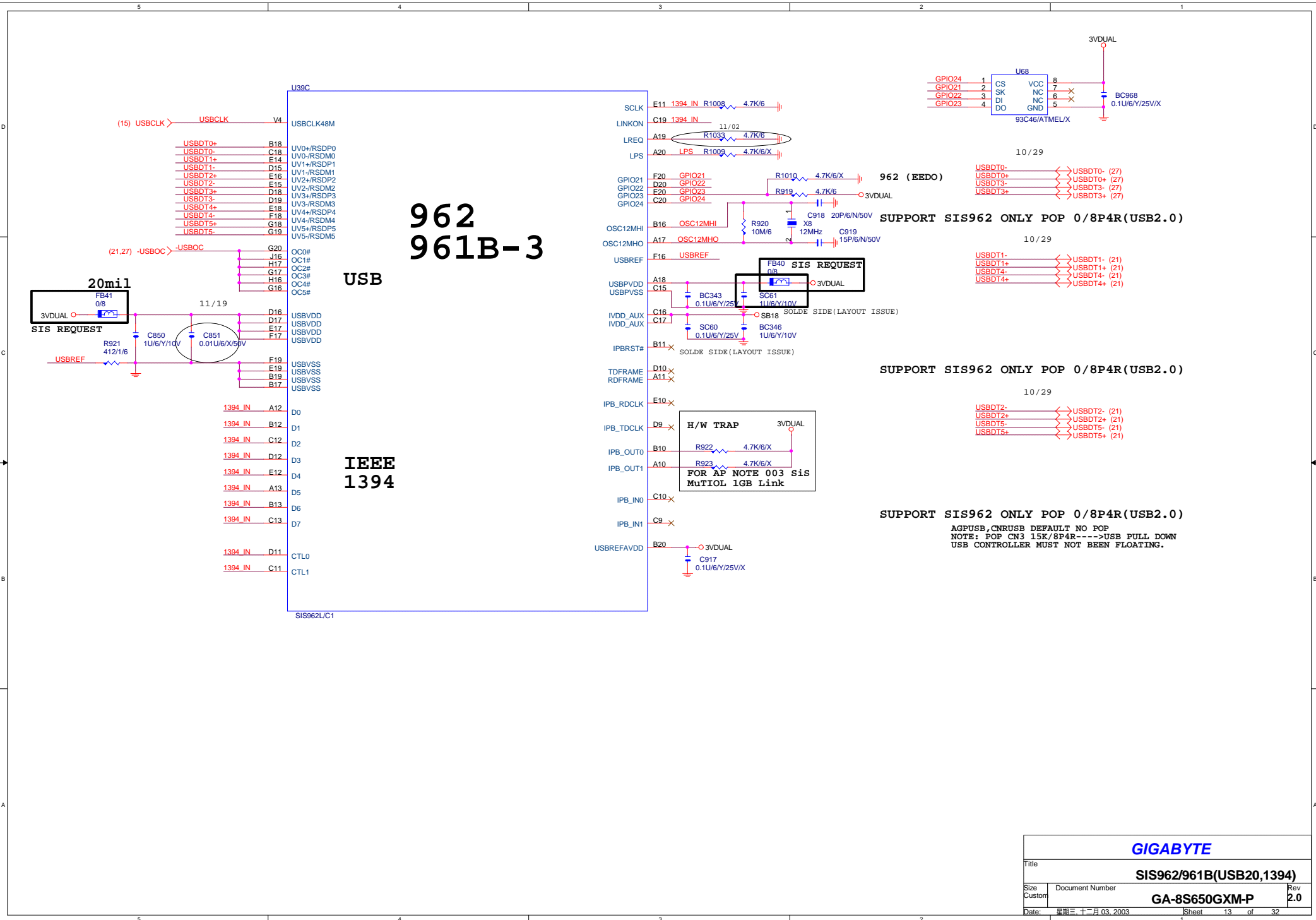
INPUT	REV:2.0/2.1	REV:3.0	
GPIO1	HI	HI	
GPIO4	LOW	LOW	
GPIO13	LOW	HI	

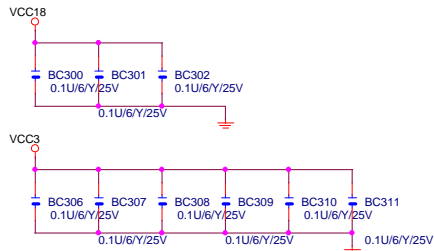
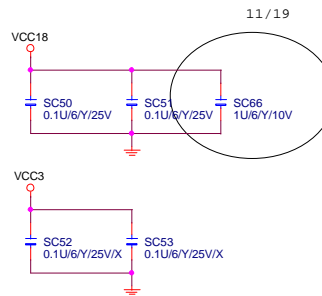
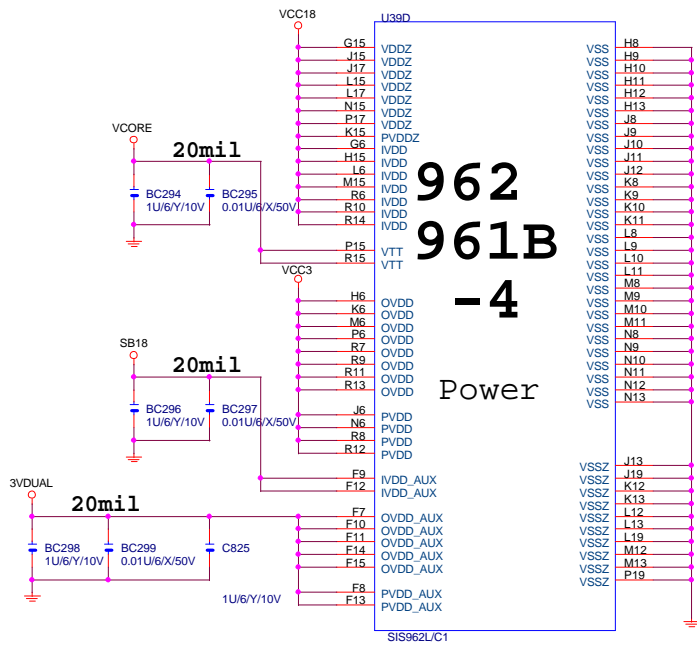
GIGABYTE

Title: **SIS962/961B(CPU,LPC,RTC,AC97,GPIO,ACPI,KBC)**

Size: Custom Document Number: **GA-8S650XM-P** Rev: **2.0**

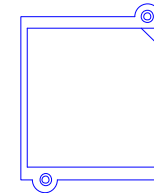
Date: 星期三, 十二月 03, 2003 Sheet 12 of 32





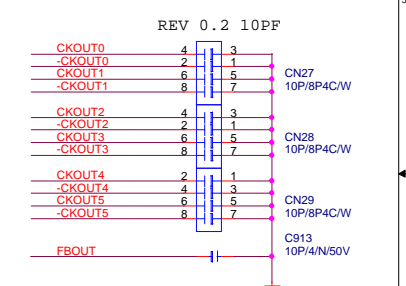
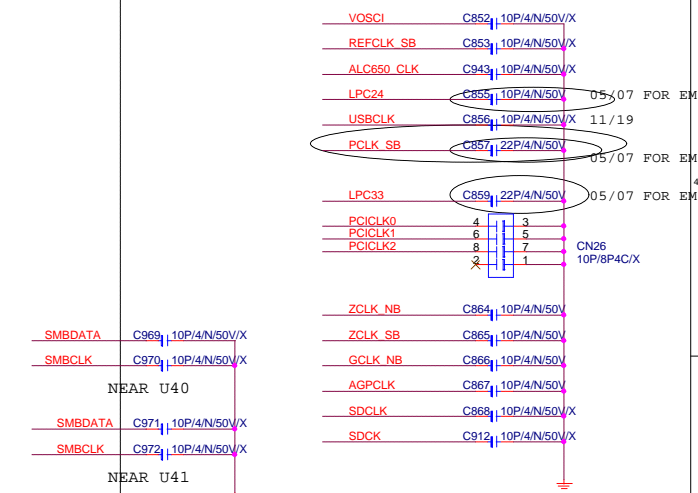
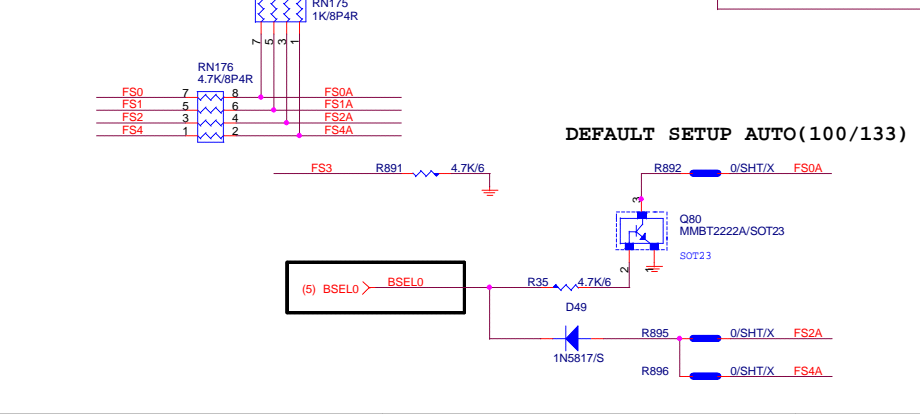
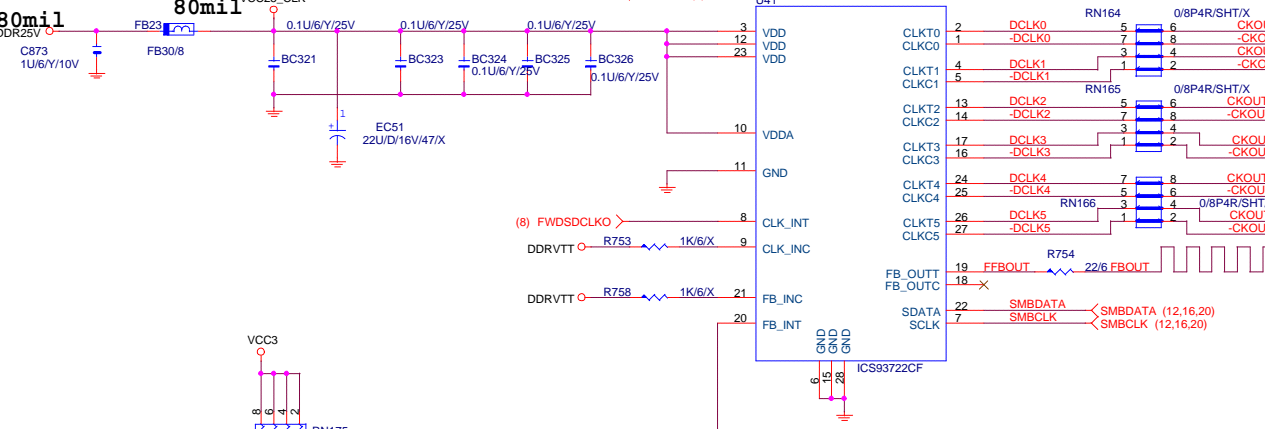
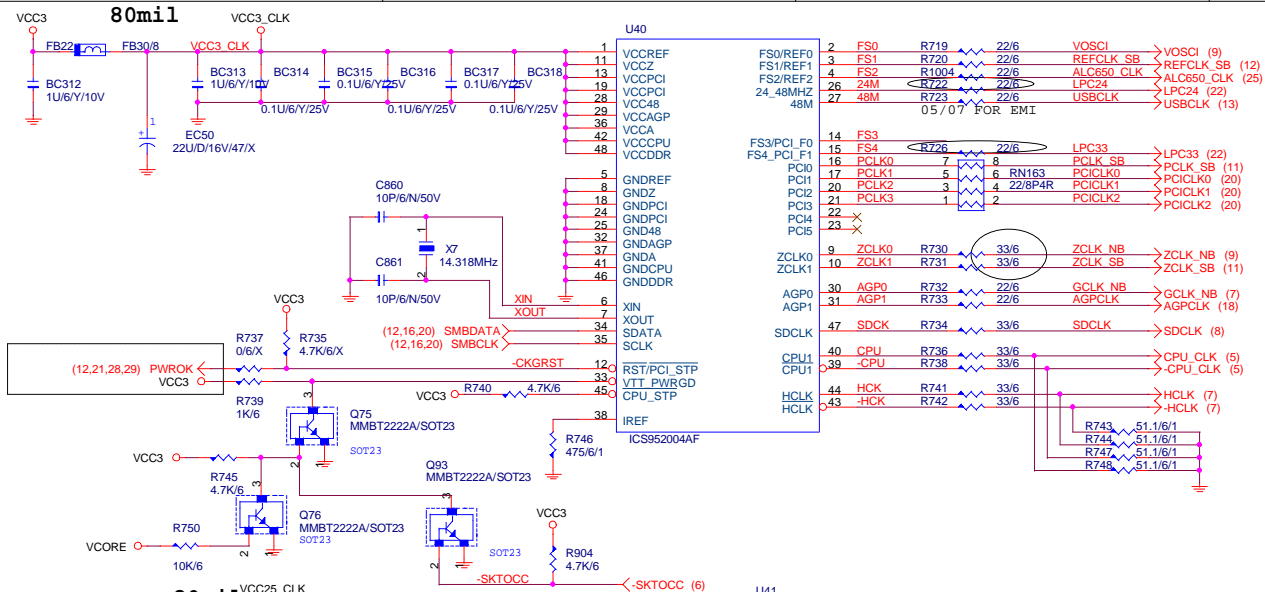
S.B HEATSINK

SB_HEATSINK1



SB_HEATSINK/X

GIGABYTE		
Title		
SIS962/961B(PWR)		
Size	Document Number	Rev
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DCLK +/----->0 ohm ADD CAP 10PF (clear glitch)

GIGABYTE

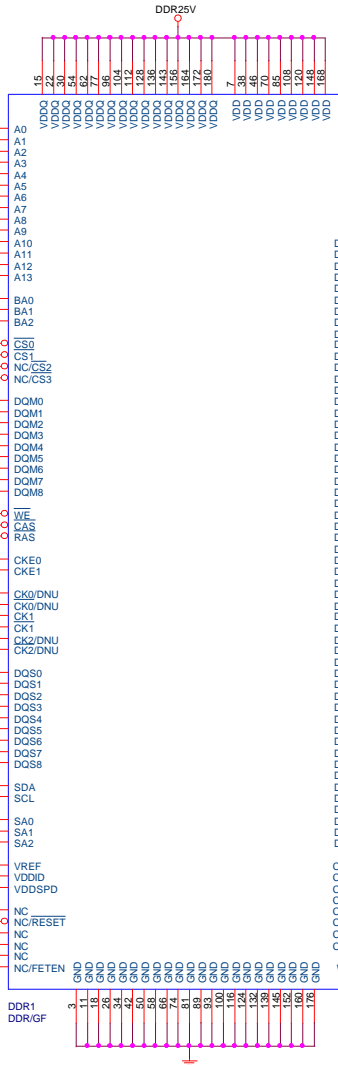
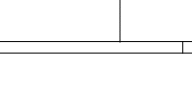
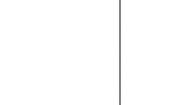
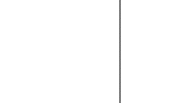
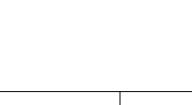
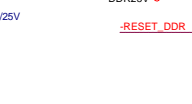
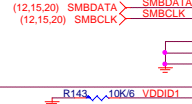
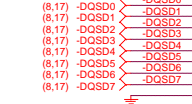
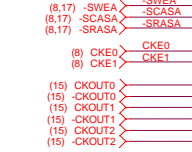
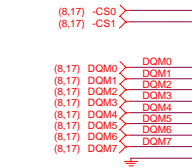
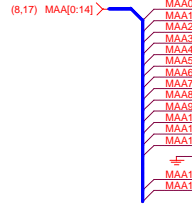
Title
CLOCK GEN + DDR BUFFER

Size Custom	Document Number	Rev 2.0
GA-8S650GX-M-P		

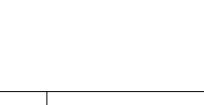
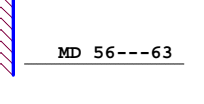
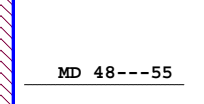
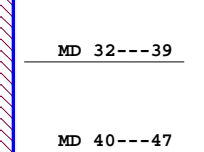
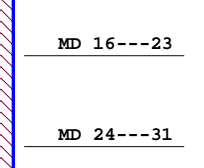
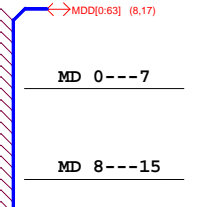
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DDR SDRAM 1,2

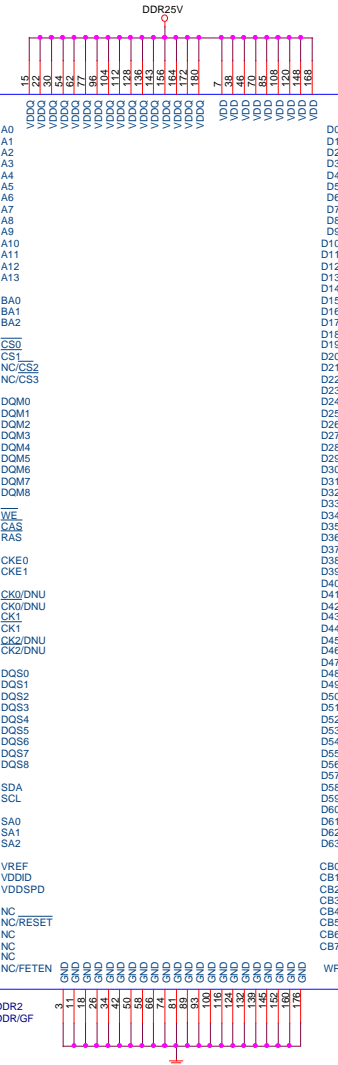
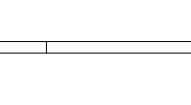
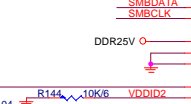
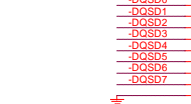
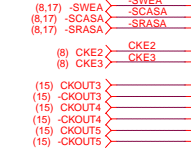
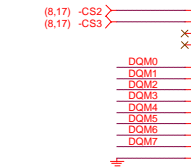
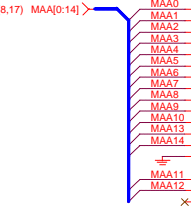
SIS ONLY MAA



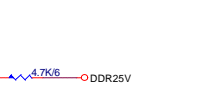
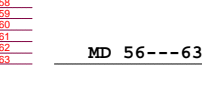
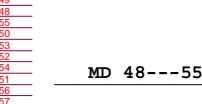
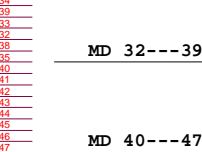
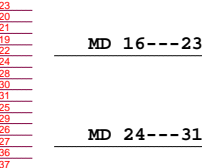
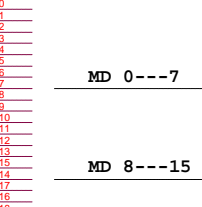
DDR MD GROUP SWAP



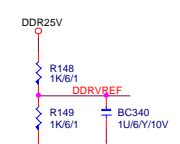
SIS ONLY MAA



DDR MD GROUP SWAP



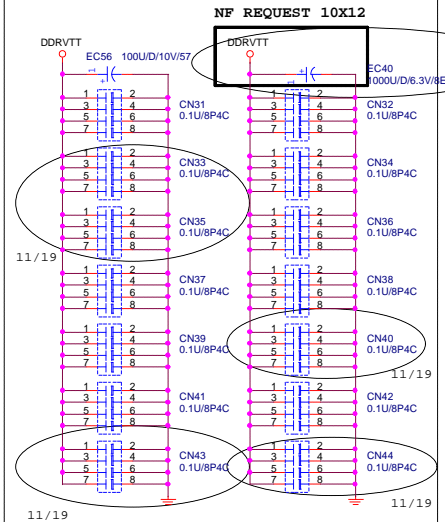
For Register DDR Support



GIGABYTE

Title			DDR UNBUFFERED 1,2
Size	Document Number	Rev	
Custom	GA-8S650GX-M-P	2.0	
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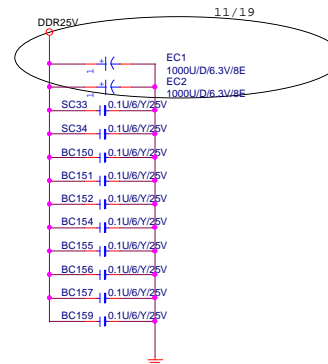
DDRVTT Decouple



R&D NOTE 109 (0.1U/8P4C X9PCS)

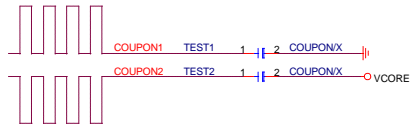
NOTE: Place these decoupling capacitors close to VTT_MEM termination resistors. (one decoupling capacitor for each two R-packs)

DDR25V Decouple



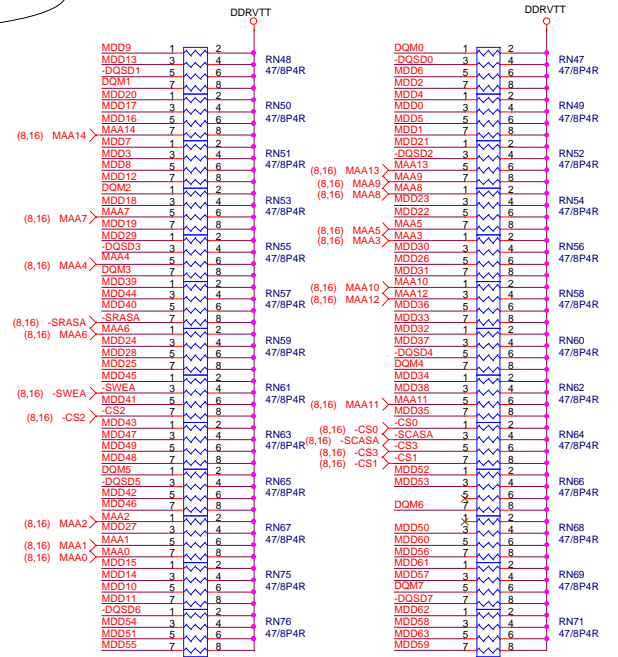
NOTE: Place Dretribute 4 pcs per DDR module.

IMPEDENCE TESTING COUPON



DDR TERMINATION

REV 0.2 DDR DIMM ISSUE
33-->47 OHM

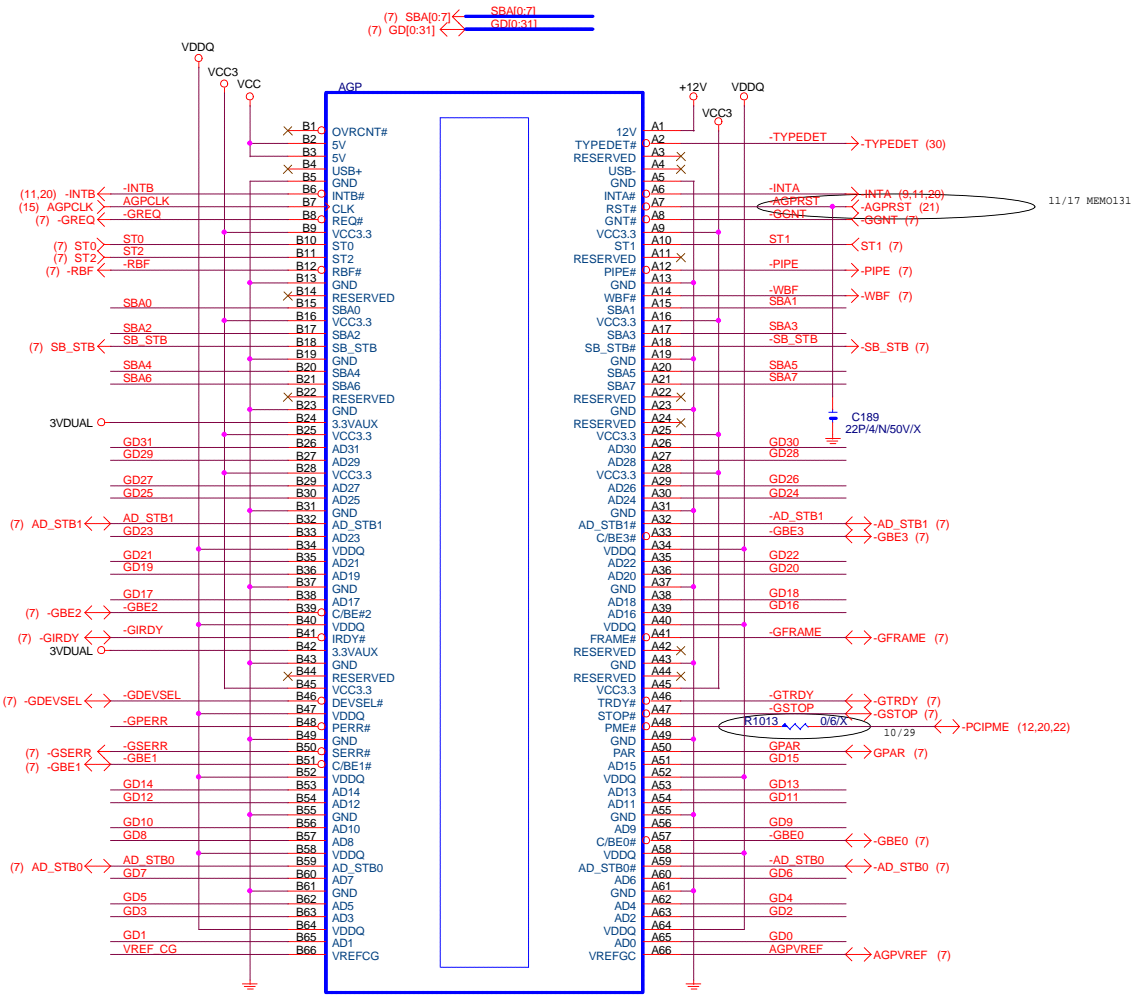


(8,16) MDD[0:63] ← MDD[0:63]

(8,16) DQM0 → DQM0
(8,16) DQM1 → DQM1
(8,16) DQM2 → DQM2
(8,16) DQM3 → DQM3
(8,16) DQM4 → DQM4
(8,16) DQM5 → DQM5
(8,16) DQM6 → DQM6
(8,16) DQM7 → DQM7

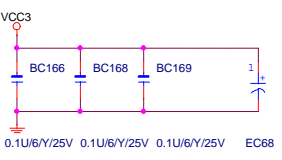
(8,16) -DQSD0 → -DQSD0
(8,16) -DQSD1 → -DQSD1
(8,16) -DQSD2 → -DQSD2
(8,16) -DQSD3 → -DQSD3
(8,16) -DQSD4 → -DQSD4
(8,16) -DQSD5 → -DQSD5
(8,16) -DQSD6 → -DQSD6
(8,16) -DQSD7 → -DQSD7

Title			
GIGABYTE			
DDR UNBUFFERED 3			
Size	Document Number	Rev	
Custom	GA-8S650GXM-P	2.0	
Date:	星期二, 十二月 03, 2003	Sheet	17 of 32

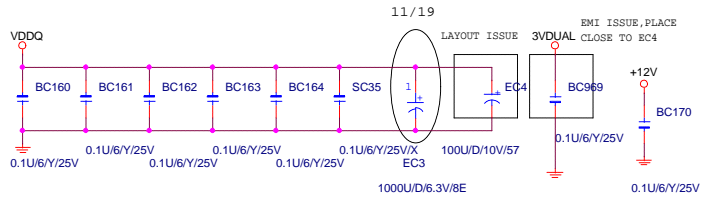


UAGP132/CO/GF
REV 0.2 AGP BOM MODIFY
11AC1-05R124-11

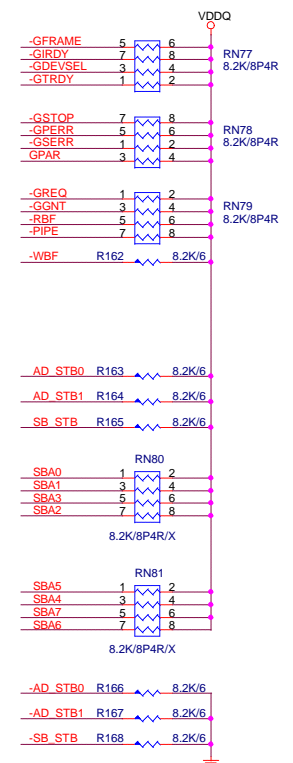
AGP SLOT (AGP-N)



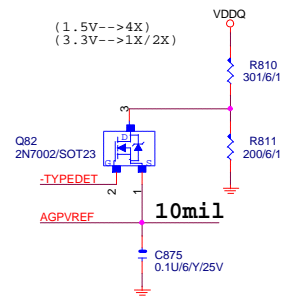
Place 1 at each pair of 3.3V pins
Decoupling capacitors
(Place near AGP slot)



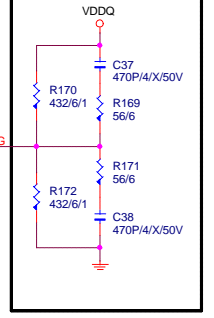
Place 1 at each pair of VDDQ pins
Place an additional for spread from A14 - A33



SWITCH CIRCUIT FOR VDDQ



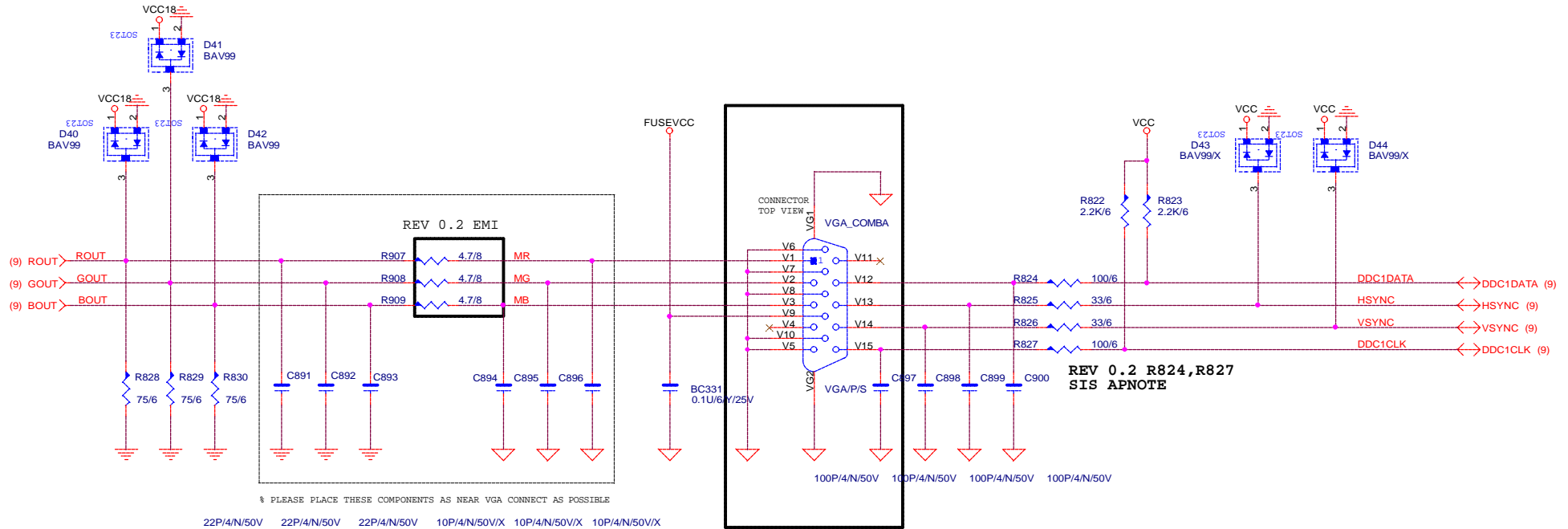
SIS DESIGN



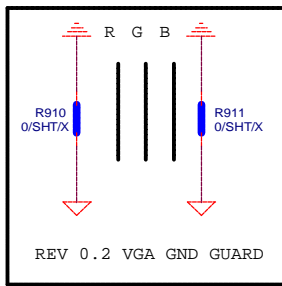
GIGABYTE		
AGP SLOT		
Title	AGP SLOT	
Size	Document Number	Rev
Custom	GA-8S650GX-M-P	2.0
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VGA CONNECTOR 1

SIS 645DX NO POP



DUAL LAYOUT (VGA/COM)



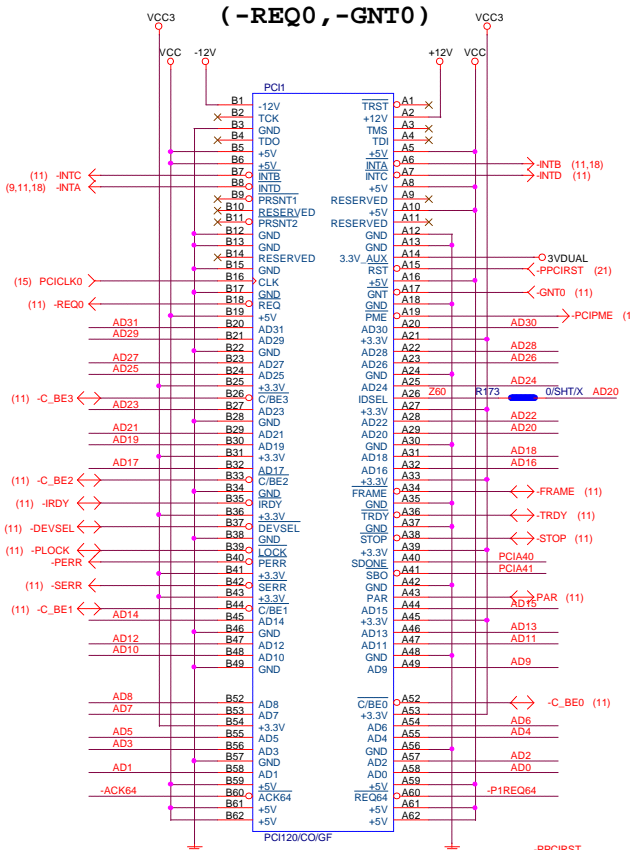
GIGABYTE		
Title VGA CONNECTOR		
Size B	Document Number GA-8S650GXM-P	Rev 2.0
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PCI SLOT 1,2,3

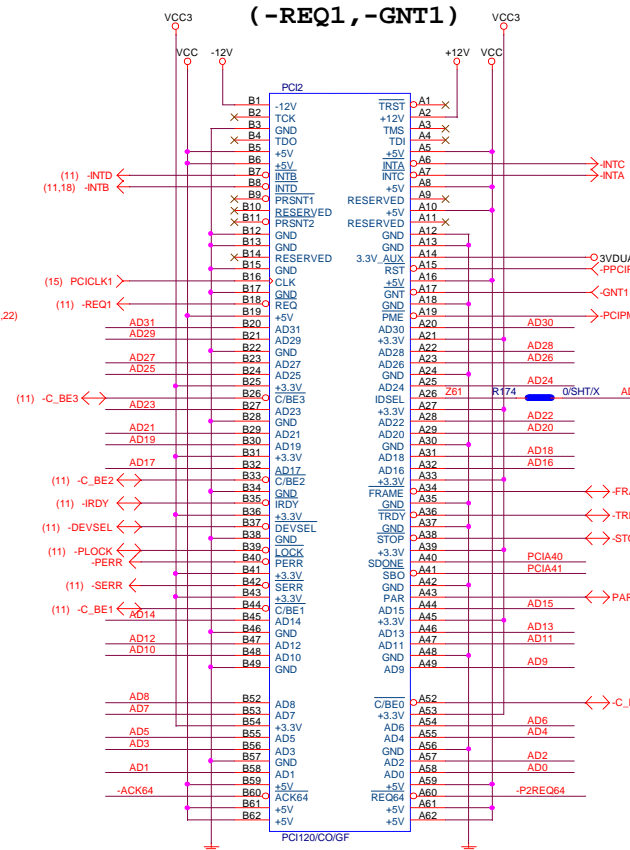
PCI SLOT1
(-REQ0, -GNT0)

PCI SLOT2
(-REQ1, -GNT1)

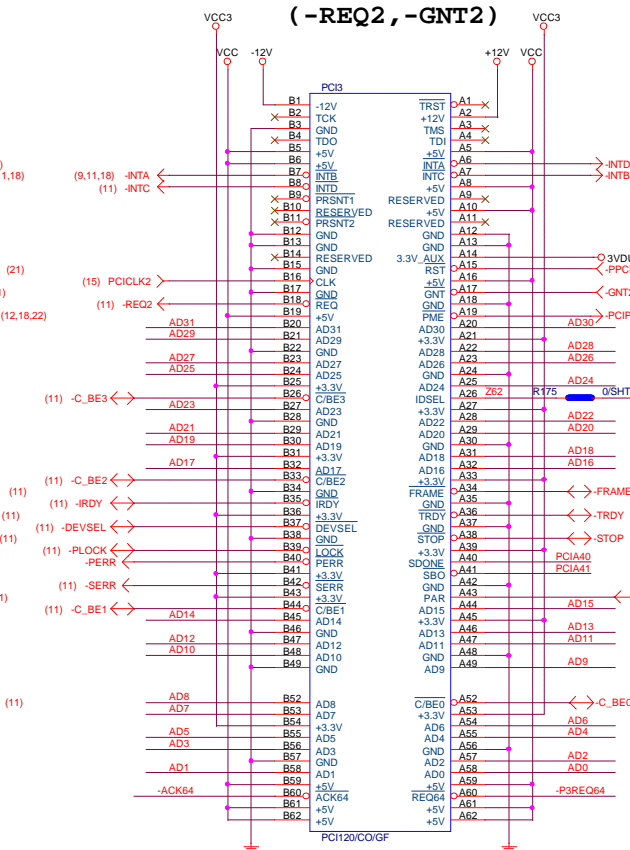
PCI SLOT3
(-REQ2, -GNT2)



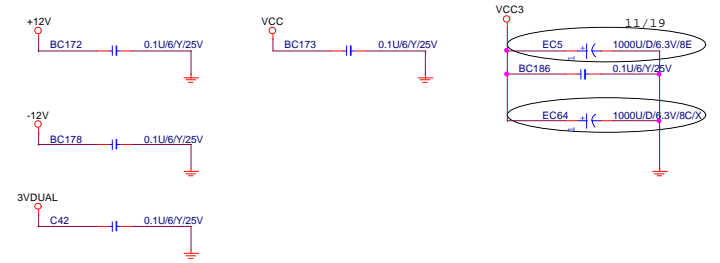
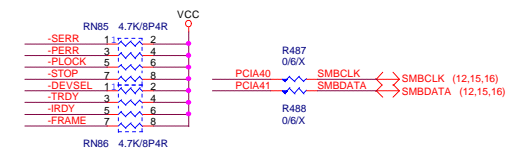
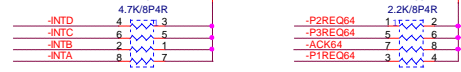
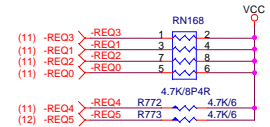
SIS-IDSEL(A20)
(B)



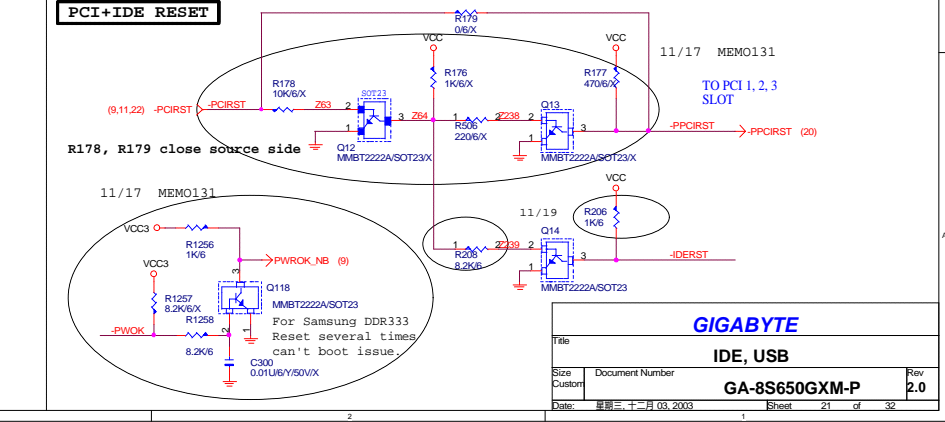
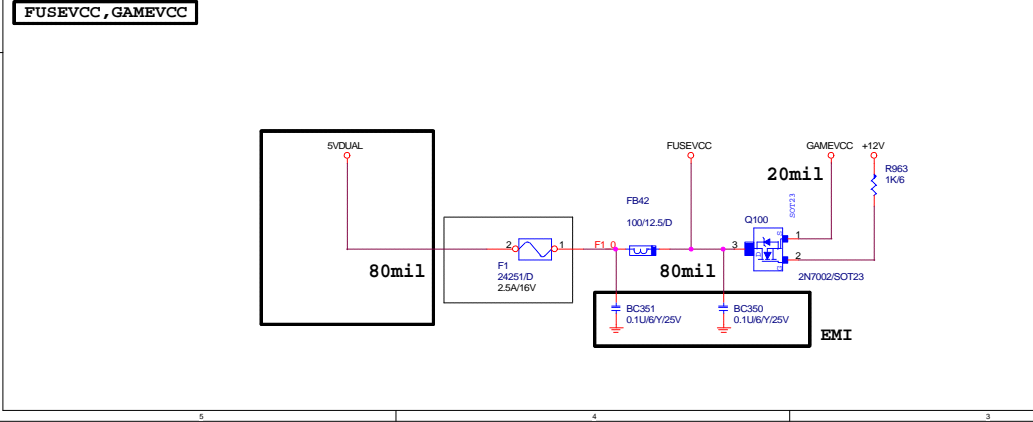
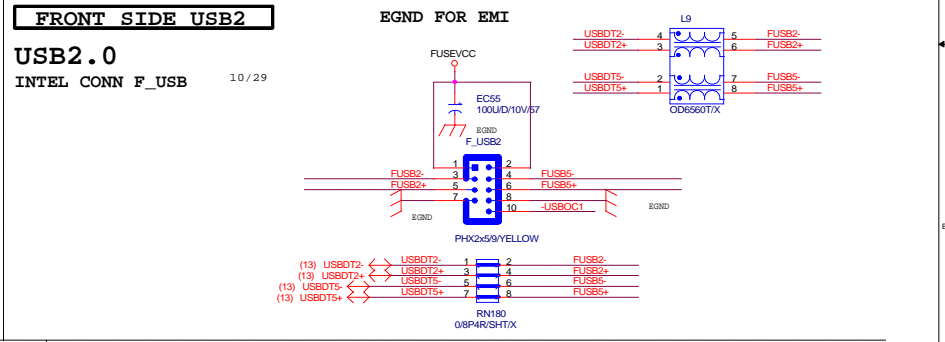
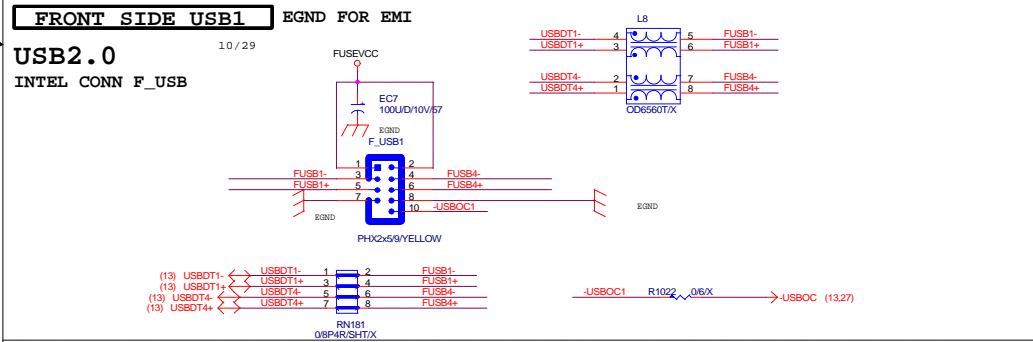
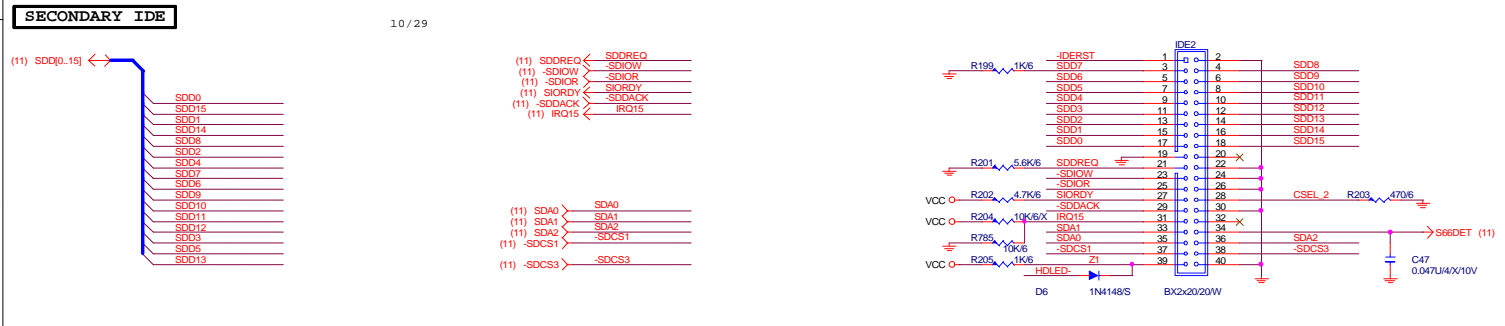
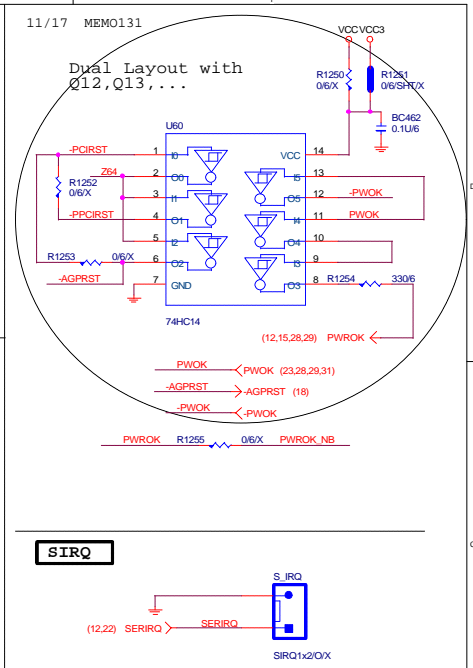
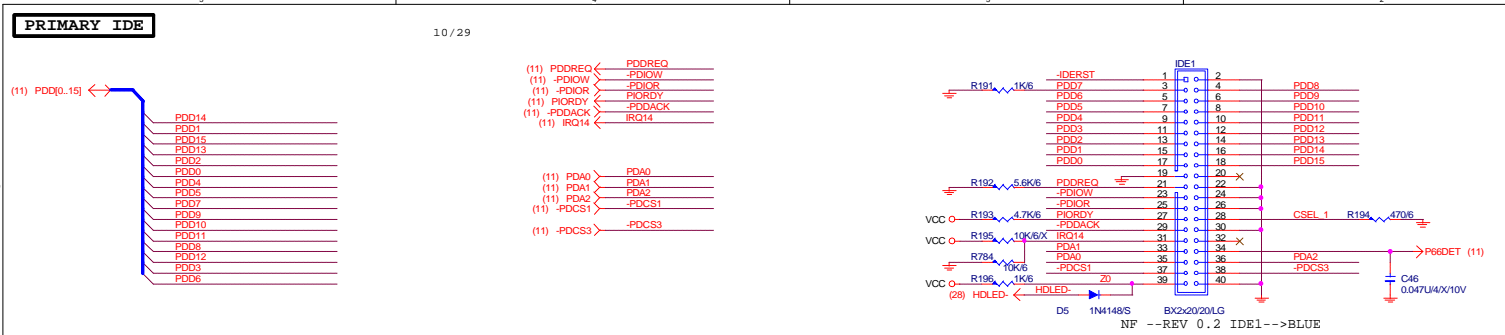
SIS-IDSEL(A22)
(C)



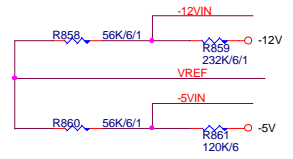
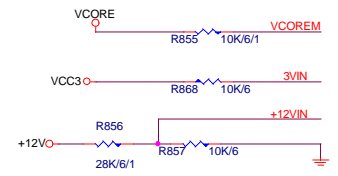
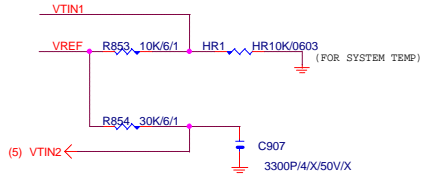
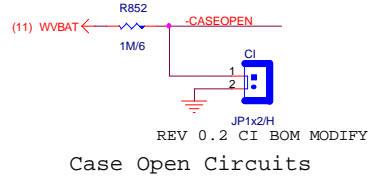
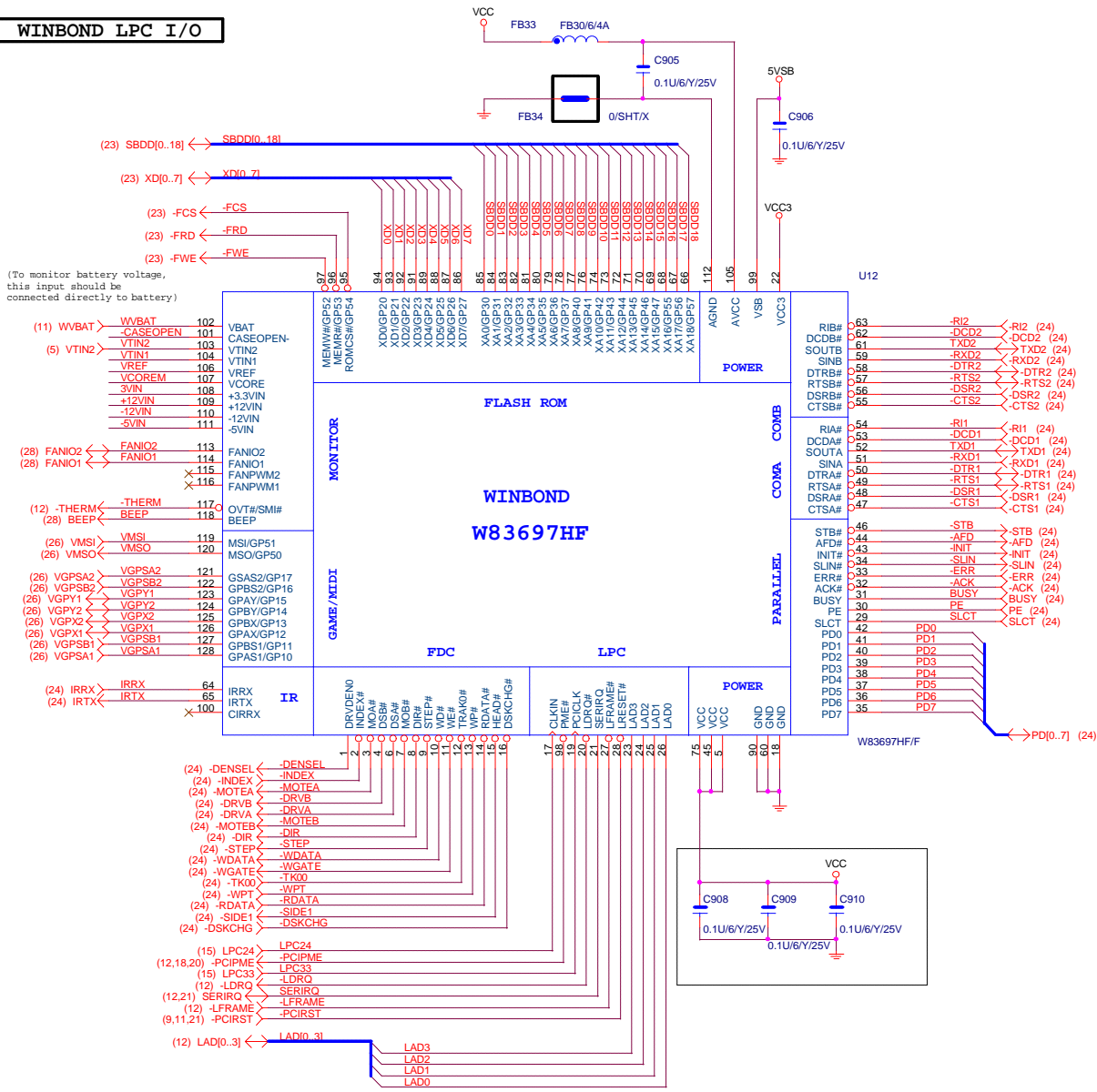
SIS-IDSEL(A24)
(D)



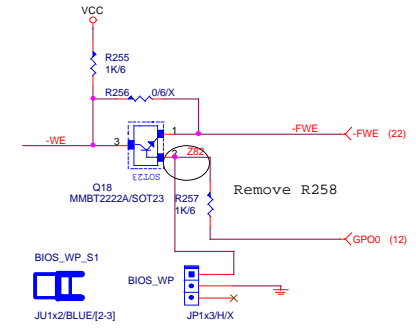
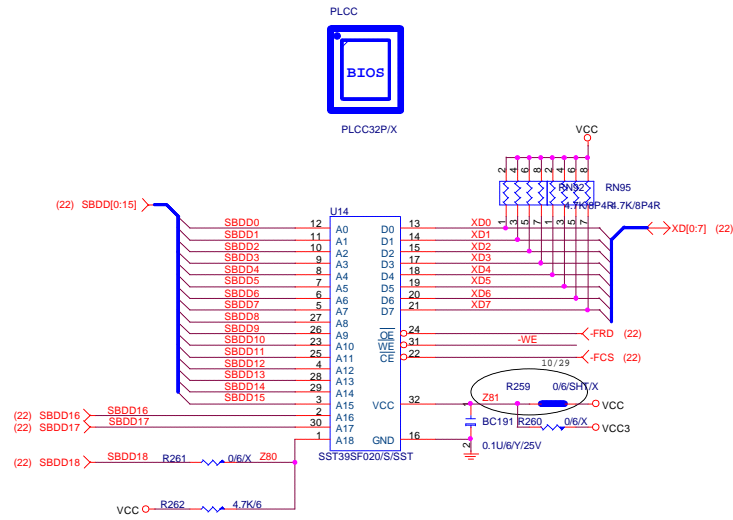
Title		
GIGABYTE		
PCI SLOT 1,2,3		
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WINBOND LPC I/O

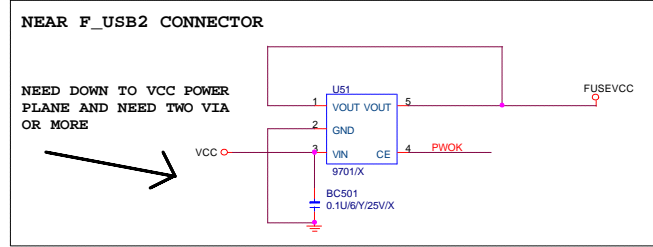
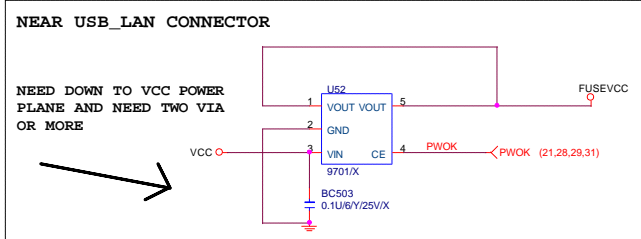
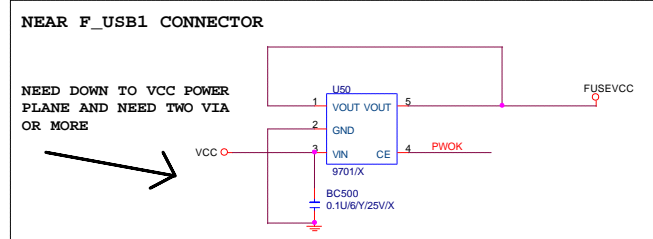


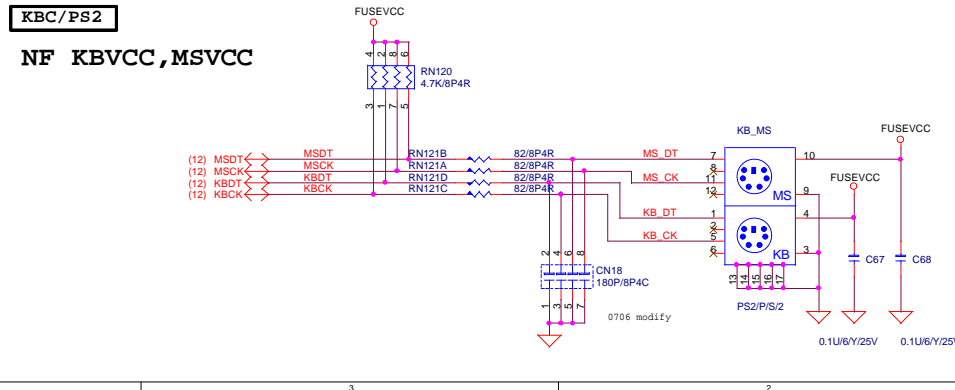
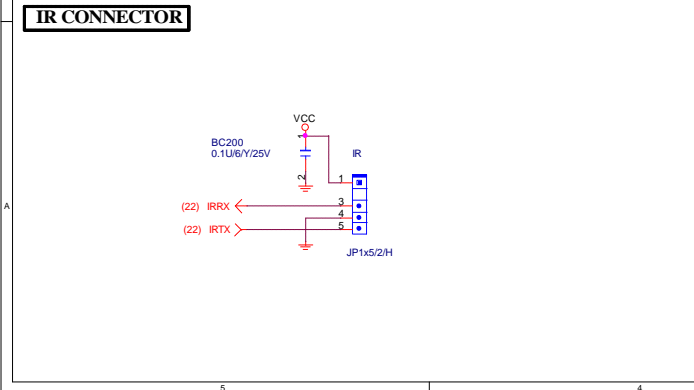
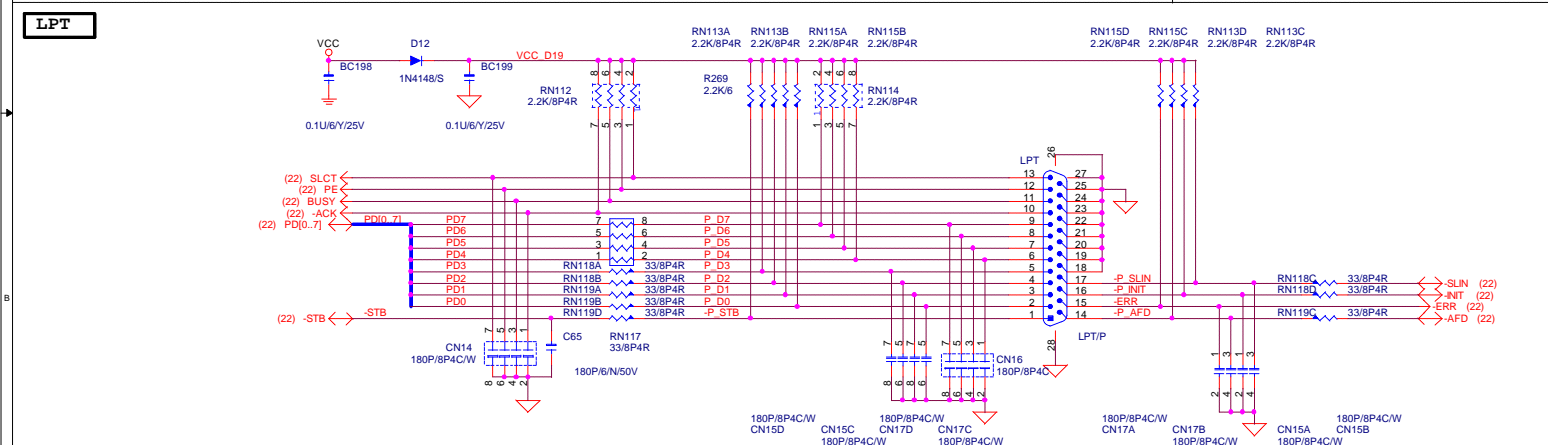
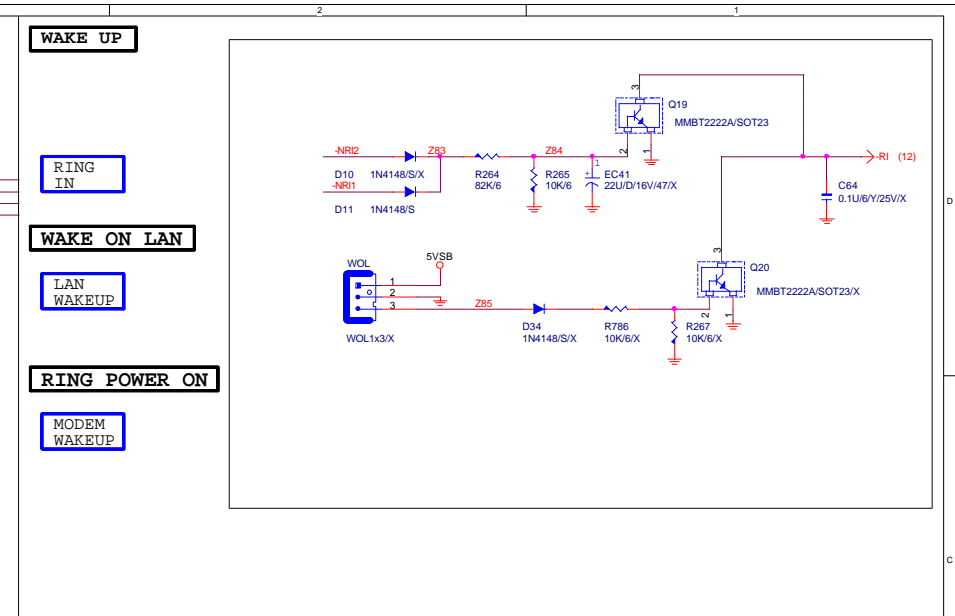
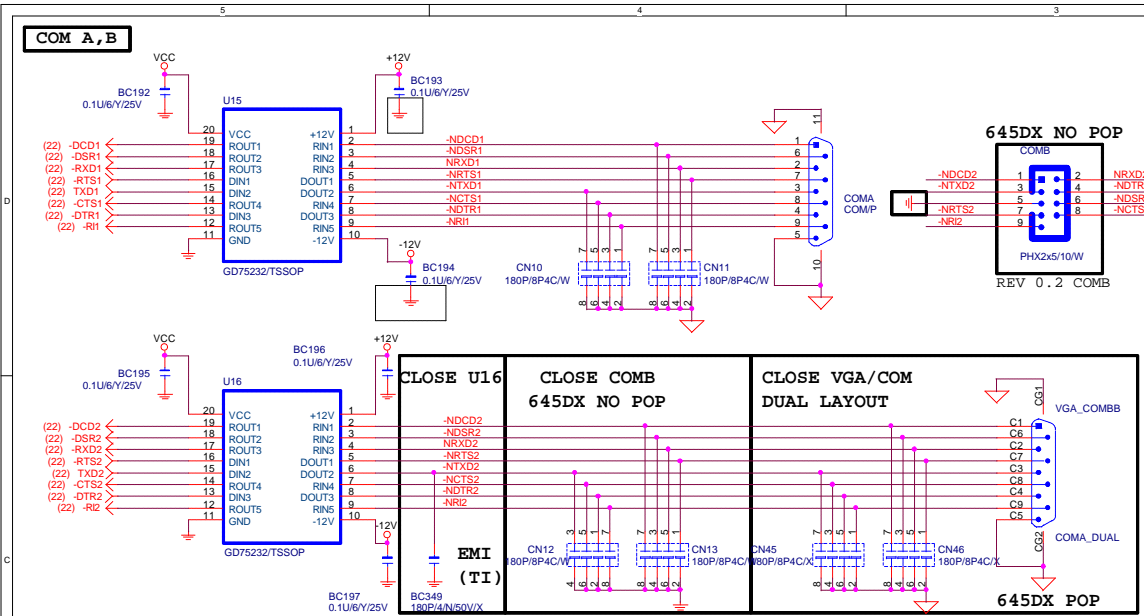
GIGABYTE		
Title		
LPC W83697		
Size	Document Number	Rev
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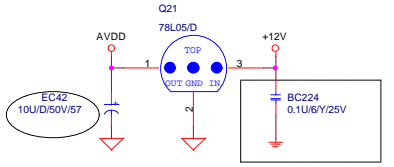
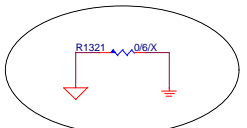
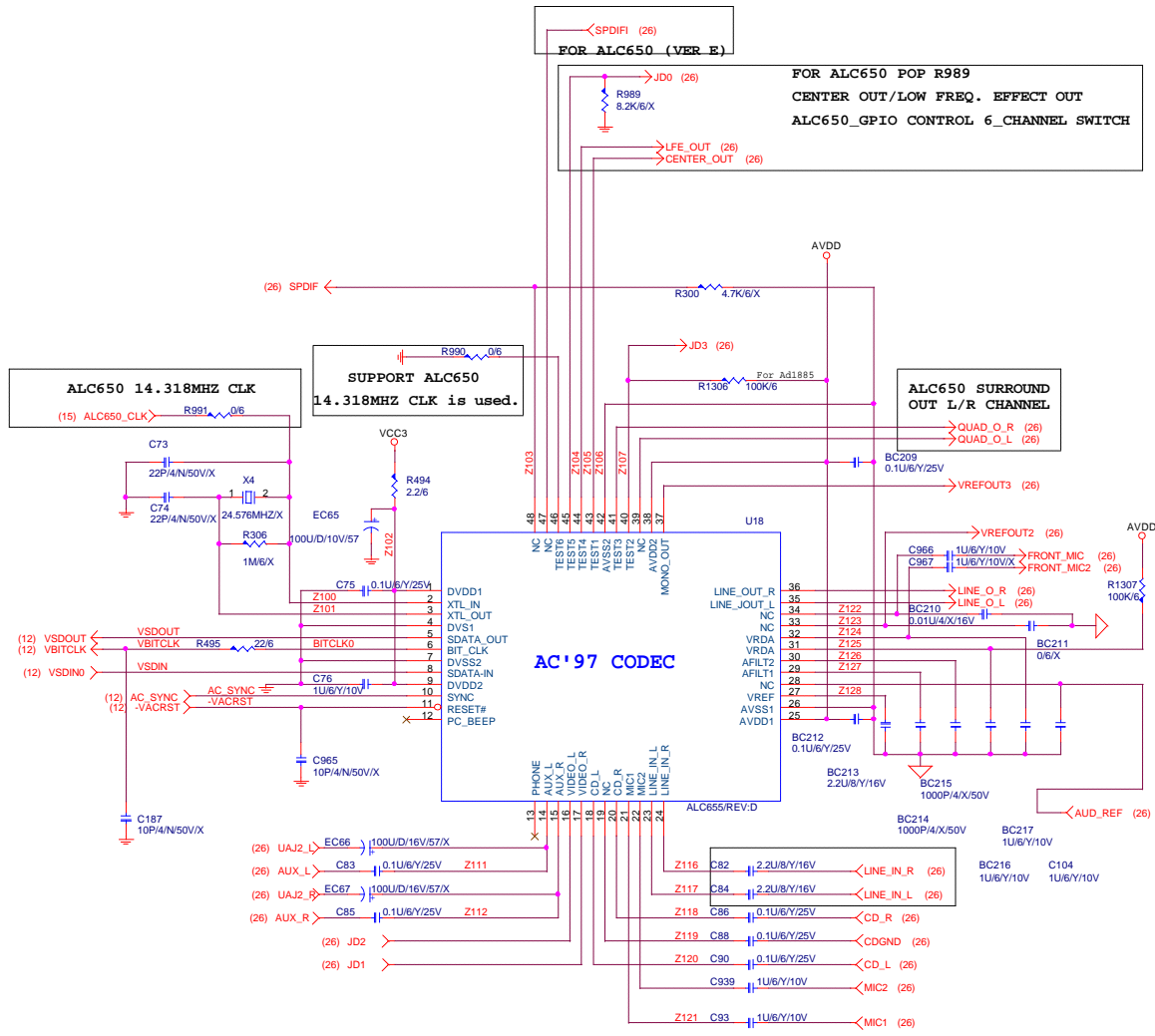
BIOS_WP: BIOS WRITE PROTECT

PIN	BIOS_WP
1-2	WRITE PROTECT
2-3	WRITE ENABLE (default)



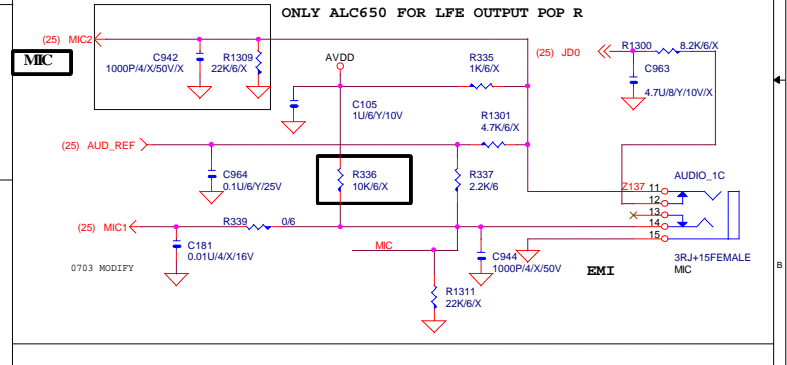
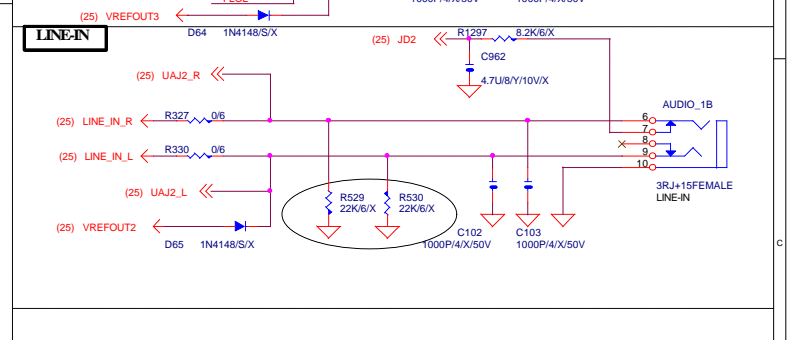
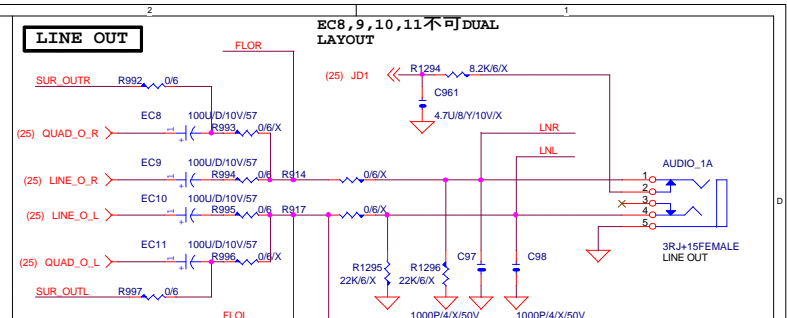
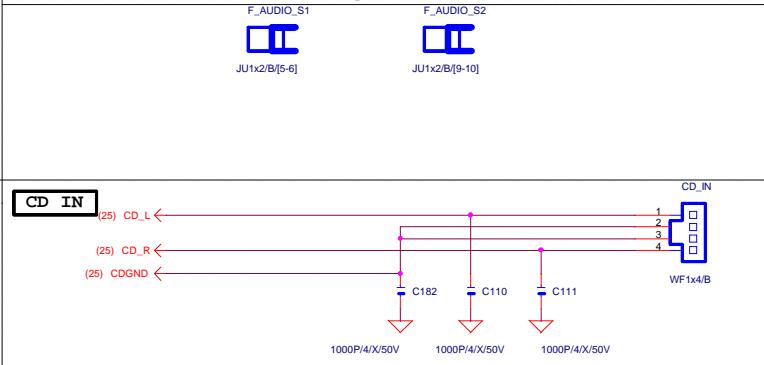
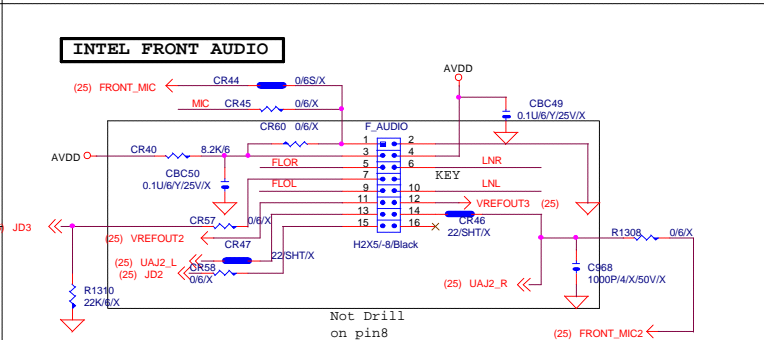
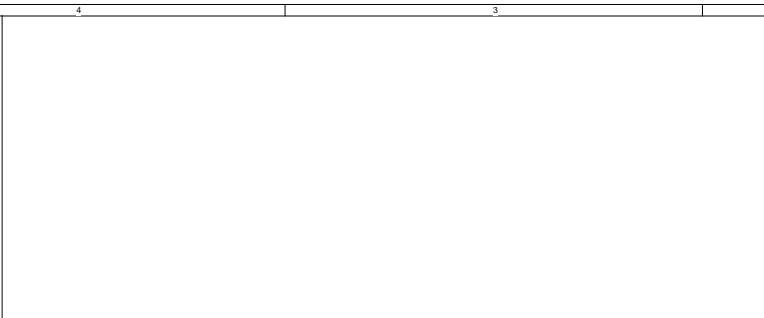
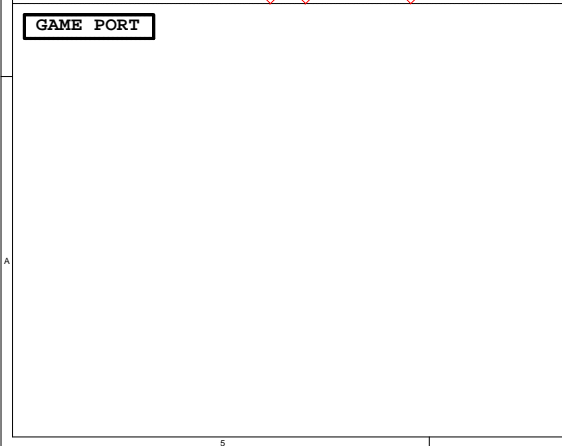
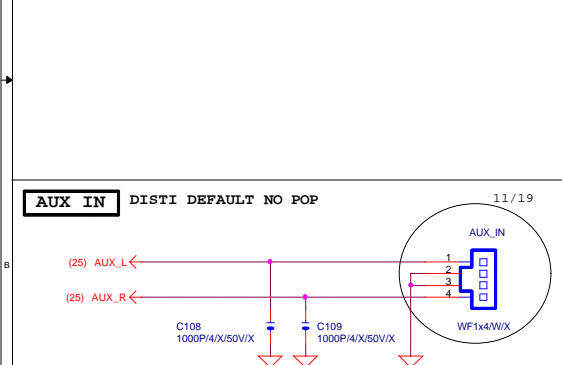
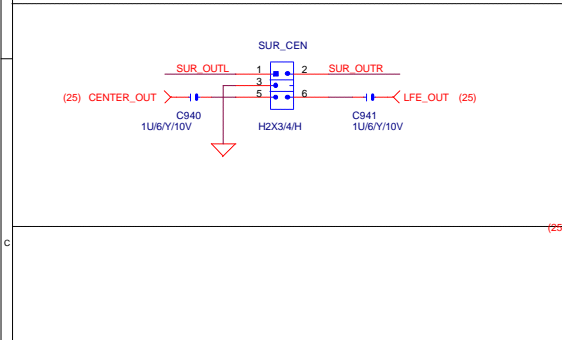
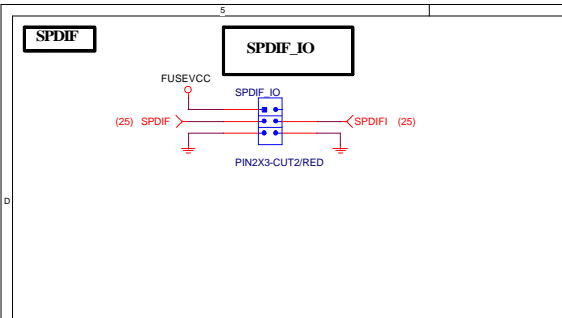


GIGABYTE			
COM,PRT,FDD,KB,IR			
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NF	SIGMATEL9756
Disti	ALC201A

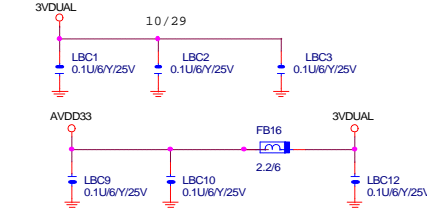
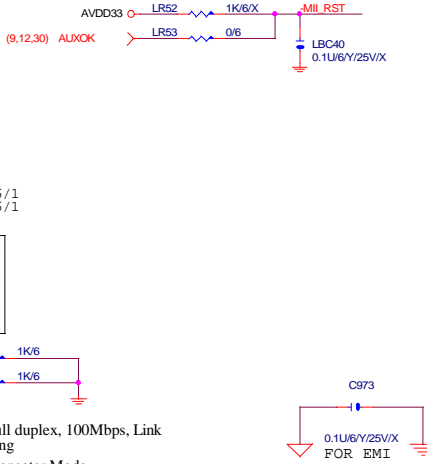
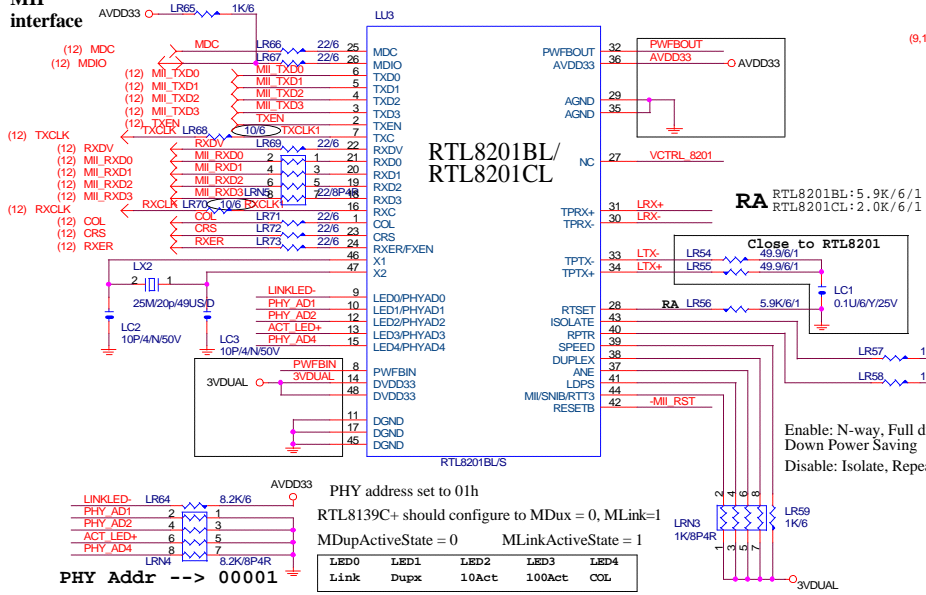
GIGABYTE			
AUDIO (AC97 CODEC)			
Title	Document Number		
Size	GA-8S650GXM-P		Rev
Custom			2.0
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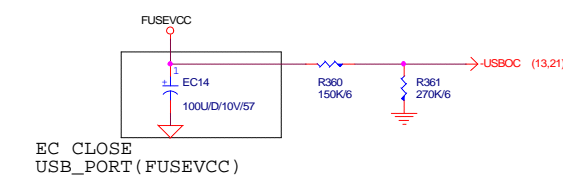
GIGABYTE			
Title			
AUDIO OUTPUT, GAME PORT			
Size	Document Number	Rev	
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Connect to MII interface

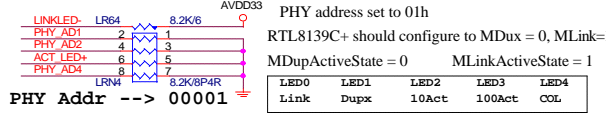
RTL8201BL/ RTL8201CL Co-Layout



USB2.0 REAR USBX2

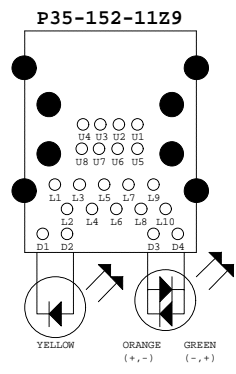


EC CLOSE
USB_PORT (FUSEVCC)

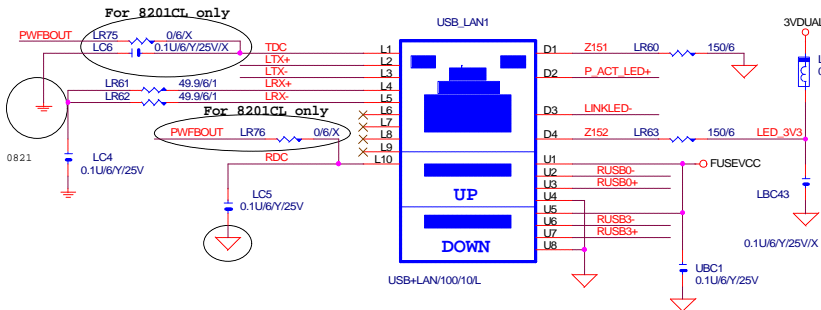
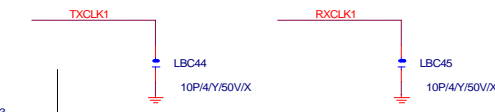
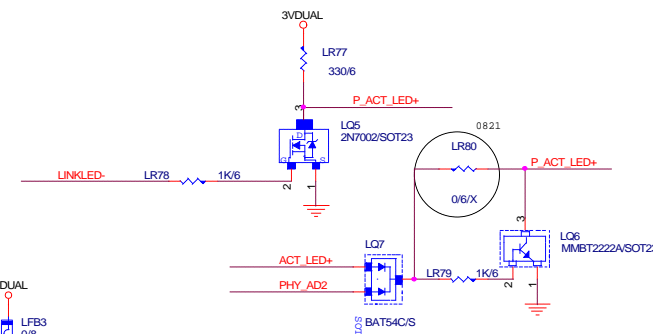
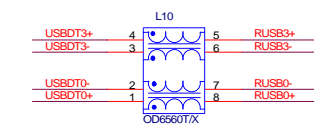
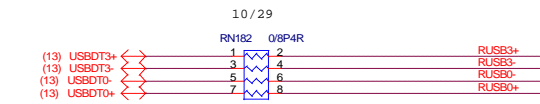
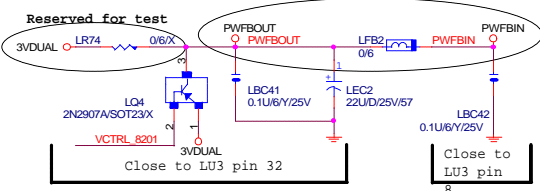
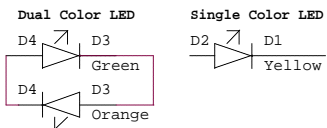


PHY address set to 01h
RTL8139C+ should configure to MDux = 0, MLink=1
MDupActiveState = 0 MLinkActiveState = 1

LED0 Link	LED1 Dupx	LED2 10Act	LED3 100Act	LED4 COL
-----------	-----------	------------	-------------	----------



Link (Speed)	Active (Data Transmit)
10Mb Green (ON)	Yellow (Blink)
100Mb Green (ON)	Yellow (Blink)
1Gb --	--

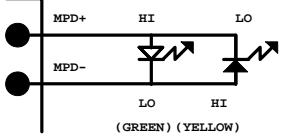


Place decoupling capacitor DC1-DC5 as close as possible to each power pin

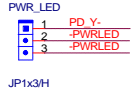
BLOCK A : The components inside BLOCK A are reserved for RTL8201B(.25u version). In RTL8201B, DVDD0 and AVDD0 will be fed 2.5V produced by BLOCK A which is functional as linear regulator and L3, R6 will be removed. In order to be layout-compatible between RTL8201 and RTL8201B, please reserve the component space and pads in your layout for future extension.

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LAN RTL8101L		
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FRONT PANEL



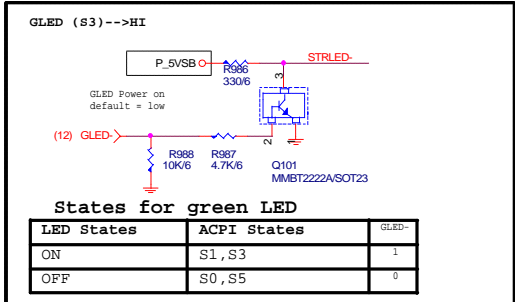
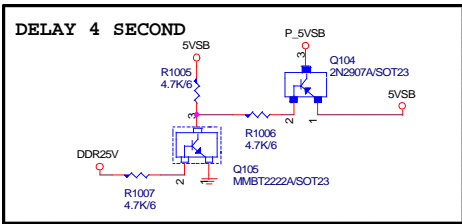
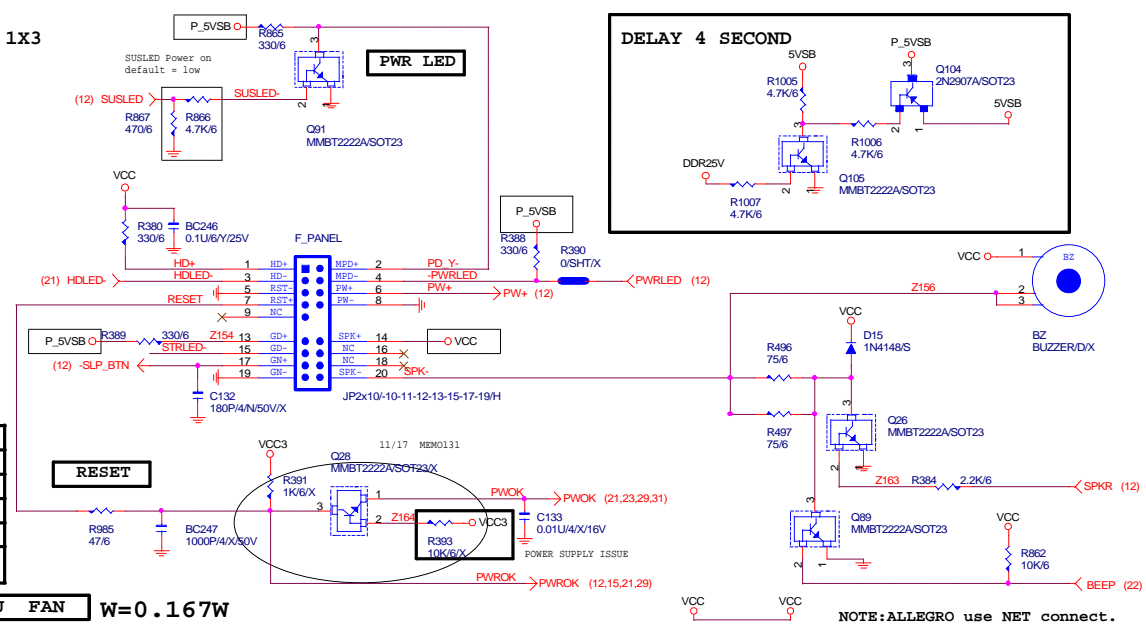
**PWR_LED FOR DISTI PIN 1X3
LED USED**



LED States	ACPI States	MPD+	MPD-
OFF	S1,S3,S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING

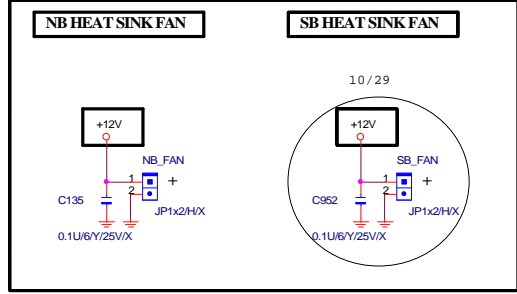
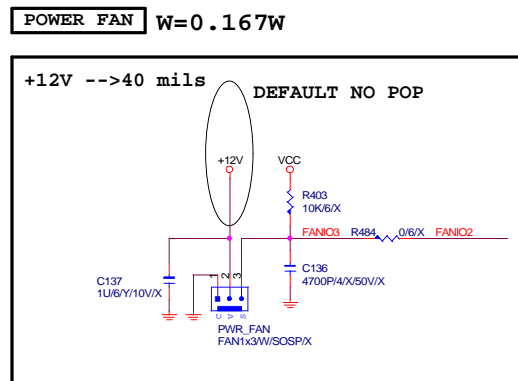
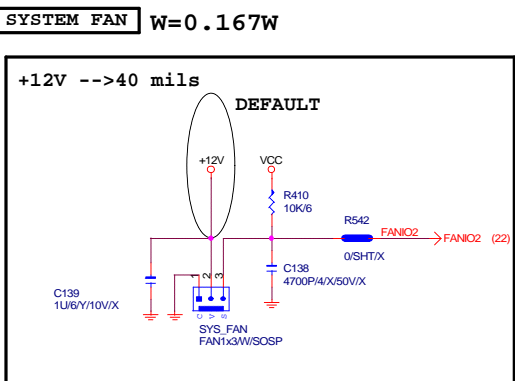
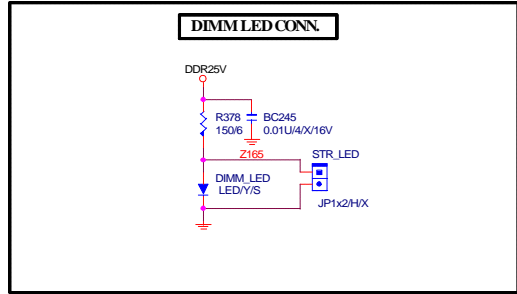
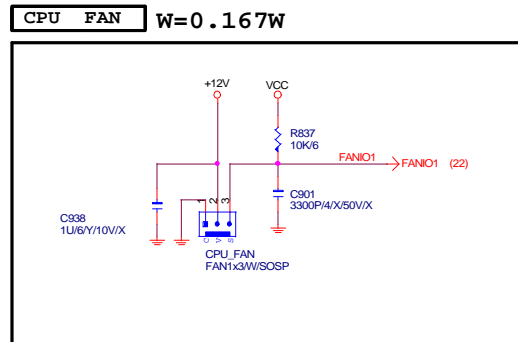
States for a dual-color power LED

LED States	ACPI States	MPD+	MPD-
OFF	S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING
Steady Yellow	S1,S3	LO	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING



States for green LED

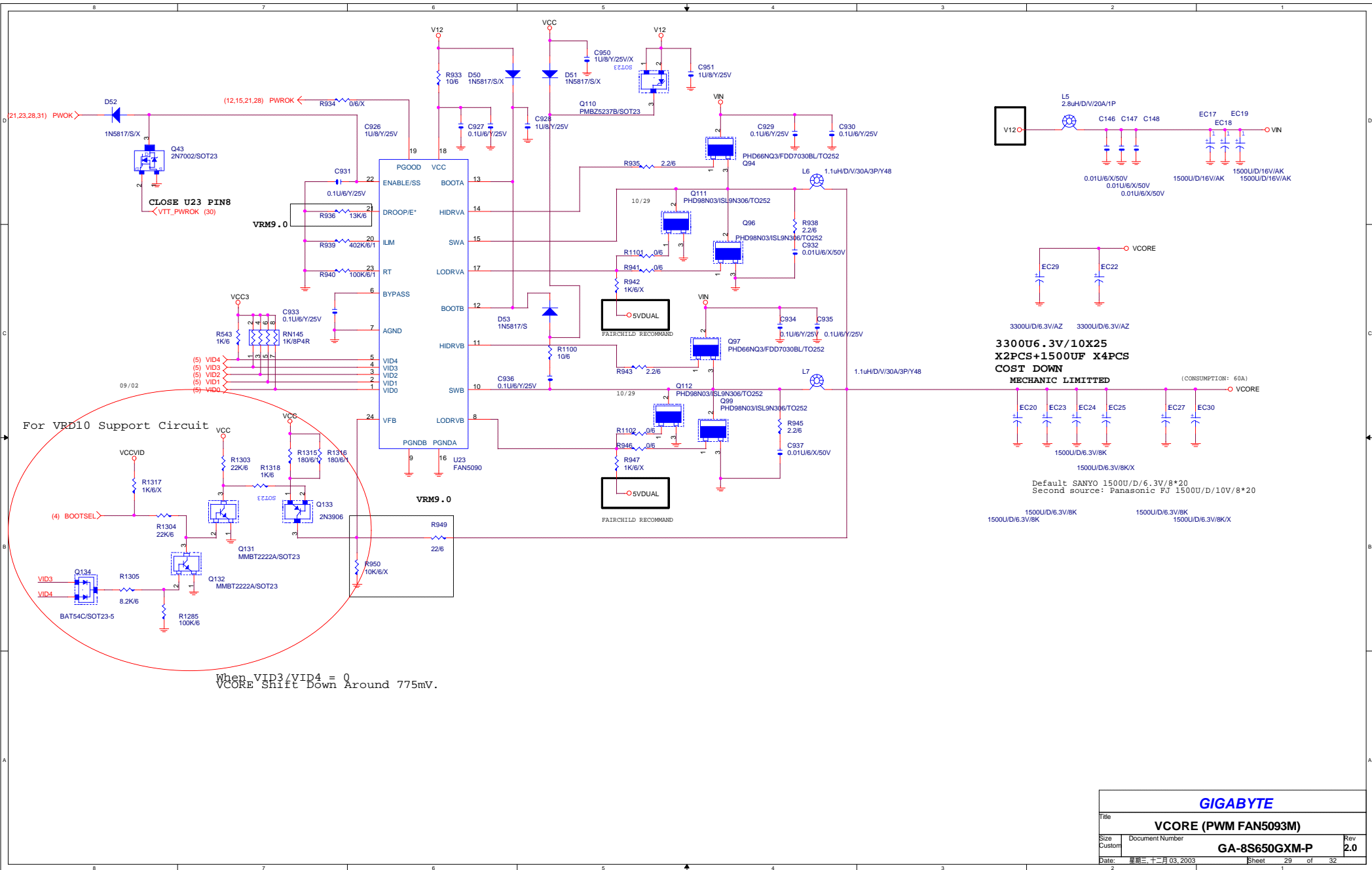
LED States	ACPI States	GLEAD-
ON	S1,S3	1
OFF	S0,S5	0



GIGABYTE

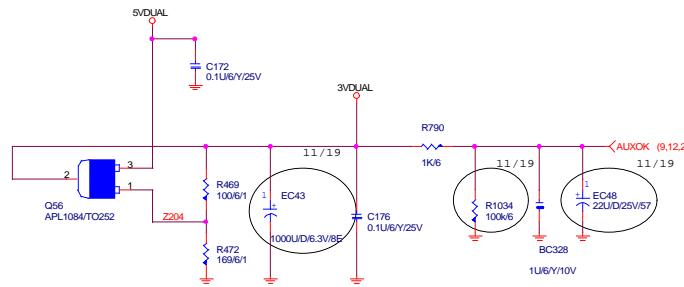
PANEL, STR LED & FANS

Title	Document Number	Rev
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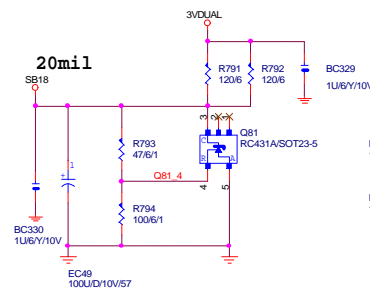
5VDUAL TRANS TO 3VDUAL(3.3V)

5VDUAL 80 mils ABOVE

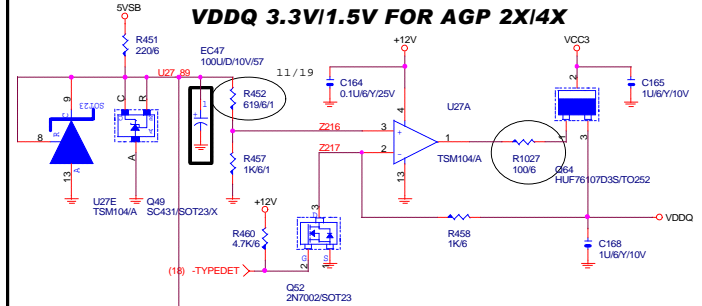


SB18 FOR SB

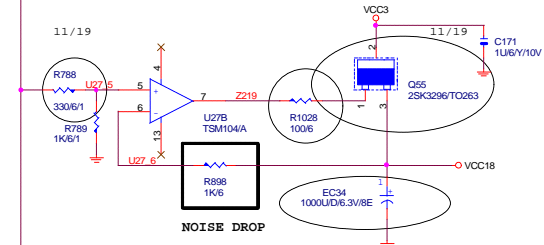
20mil



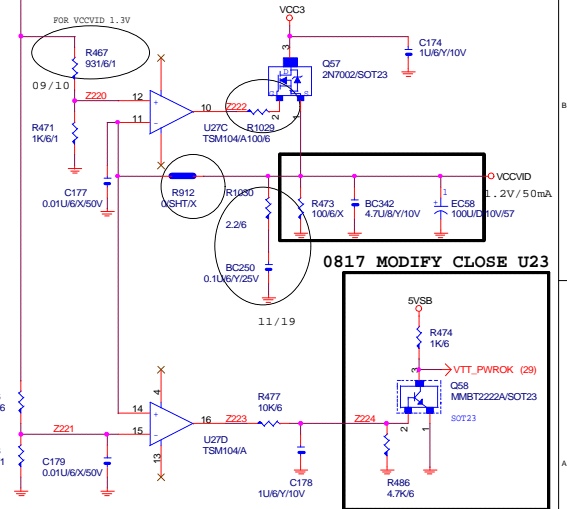
VDDQ 3.3V/1.5V FOR AGP 2X/4X



VCC18 FOR NB,SB



VCCVID FOR NORTHWOOD CPU

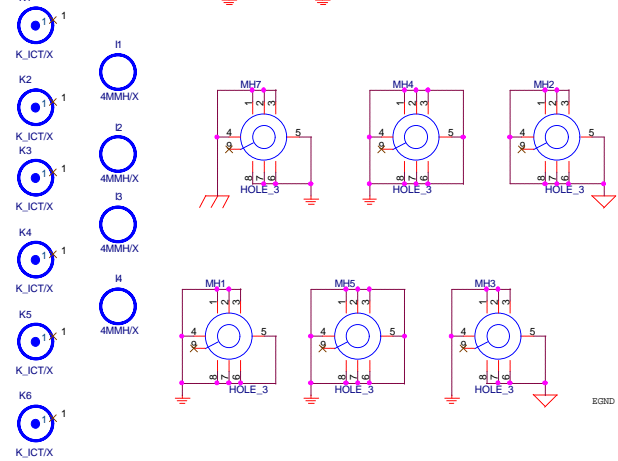
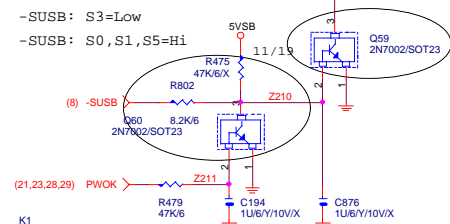
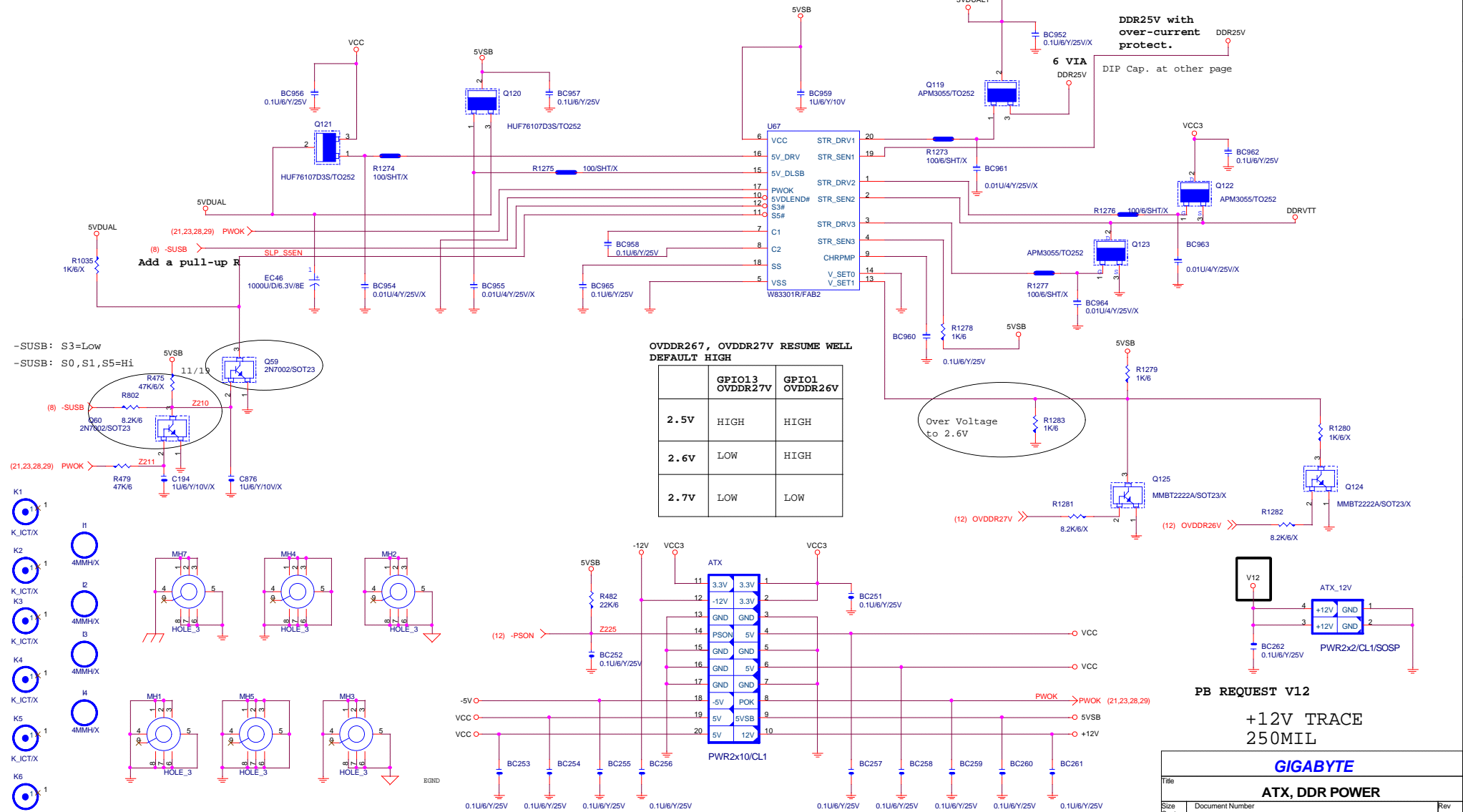
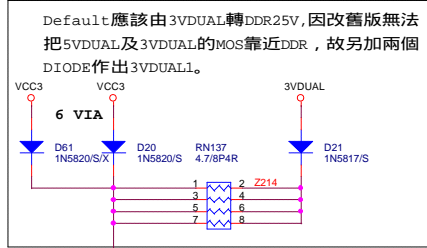


0817 MODIFY CLOSE U23

GIGABYTE		
DC POWER		
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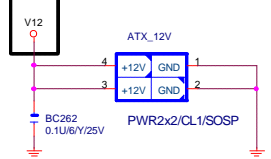
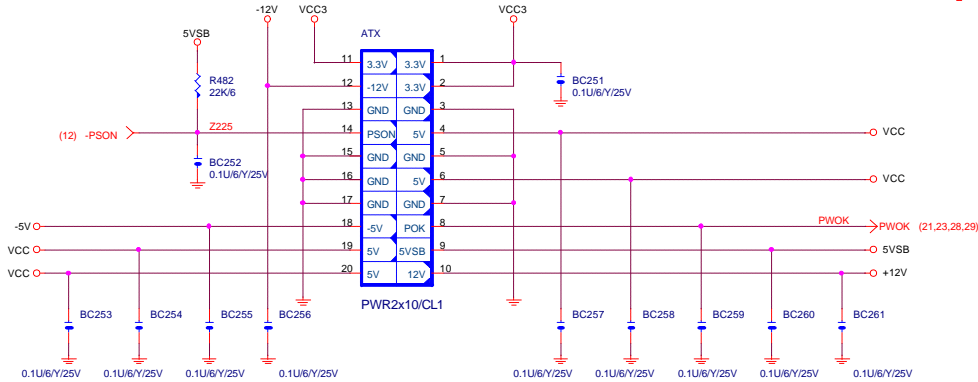
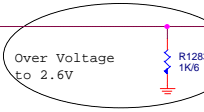
ATX CON, DDR POWER

10/29



OVD267, OVD27V RESUME WELL DEFAULT HIGH

	GPIO13 OVD27V	GPIO1 OVD26V
2.5V	HIGH	HIGH
2.6V	LOW	HIGH
2.7V	LOW	LOW



PB REQUEST V12

+12V TRACE
250MIL

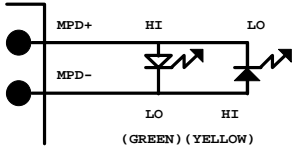
ATX POWER CONNECTOR

Title		
ATX, DDR POWER		
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LO:Normal

RTL8100L ON-BOARD			
-REQ0	PCI1	IDSEL(A20)--B	
-REQ1	PCI2	IDSEL(A22)--C	
-REQ2	PCI3	IDSEL(A24)--D	
-REQ3	RTL8100L	IDSEL(A27)--B	

8SRXL South Bridge GPIO LIST					
ITEM	DESCRIPTION	I/O	STATUS	Default	
GPIO0	Bios Write Protect	O	Hi:Write Enable, Lo:Write Protect	Hi	
GPIO1	N/A		PULL-UP	Hi	
GPIO2	THERM#			Hi	
GPIO3	Green Button	O	Hi:Normal, Lo:Into Green mode	Hi	
GPIO4	CLKRUN#		PULL-DOWN	Lo	
GPIO5	N/A		PULL-UP	Hi	
GPIO6	DDR OVER VOLTAGE	O		Hi	
GPIO7	SUSLED	O	AS LIKE DEFINED...	Lo	
GPIO8	Wake On Ring	I	Hi:Normal, Lo:Ring Power On	Hi	
GPIO9	GLED	I	AS LIKE DEFINED...	Lo	
GPIO10	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo	
GPIO11	N/A		PULL-UP	Hi	
GPIO12	N/A		PULL-UP	Hi	
GPIO13	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo	
GPIO14	DDR OVER VOLTAGE	I		Lo	
GPIO15	KB Data	I/OD			
GPIO16	KB Clk	I/OD			
GPIO17	MS Data	I/OD			
GPIO18	MS Clk	I/OD			



States for a single-color power LED

LED States	ACPI States	MPD+	MPD-	BIOS	
				GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING

States for a dual-color power LED

LED States	ACPI States	MPD+	MPD-	BIOS	
				GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING
Steady Yellow	S1,S3	LO	HI	HI	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING	HI	BLINKING

States for green LED

LED States	ACPI States	GLED-	BIOS
			GPIO9
ON	S1,S3	HI	HI
OFF	S0,S5	LO	LO

BIOS REQUEST

SINGLE	DUAL	INTEL LED DEFINED				GIGABYTE LED DEFINED				SINGLE	DUAL
		GPIO7	ACPILED	GPIO9		GPIO7	ACPILED	GPIO9			
GREEN	GREEN	S0	LO	LO	LO	S0	LO	LO	LO	GREEN	GREEN
OFF	YELLOW	S1	HI	HI	HI	S1	LO	BLINKING	HI	G(BLINK)	G(BLINK)
OFF	YELLOW	S3	HI	HI	HI	S3	HI	HI	HI	OFF	YELLOW
OFF	OFF	S4/S5	LO	HI/NC	LO	S4/S5	LO	HI/NC	LO	OFF	OFF

GIGABYTE

Title			
GPIO, REQ/GNT Table			
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